Designing reliable analog circuits in an unreliable world

Georges Gielen
ESAT–MICAS, KU Leuven
gielen@esat.kuleuven.be
MICAS: the numbers

- **research focus** on IC design, incl. CAD

- **6 full-time professors**
  - 3 are Fellow of IEEE
  - ~55 Ph.D. students (@ ESAT)
  - ~25 Ph.D. students (@ IMEC)

- **4 affiliated professors**

- **9.5 tech/ admin staff**

- **created 6 spinoffs in last 14 years**

---

**Contents**

- **Motivation**
- Aging modeling
- Reliability simulation
- Reliability-aware or resilient design
- Conclusions
Evolution in technology

- traditional scaling philosophy: more for less

Result of scaling

- same function, smaller, faster, less power
Good news from Intel & co

CMOS scaling will continue for at least two more technology nodes beyond 32 nm!!

Variability

line edge roughness (LER)  random dopant fluctuations (RDF)

[Frank, IBM]
Analog circuits and matching

- mismatch inversely proportional to area:
  \[ \sigma^2(\Delta V) \approx \frac{A_{VT}}{WL} \]

\[ P = 24 C_{ax} A_{VT}^2 f DR^2 \]

\[ \frac{\text{Speed} \times \text{Accuracy}^2}{\text{Power}} = \text{techn const} \]

[Vittoz AICSP 1994] [Kinget CICC 1996]

Benefit from process scaling?

analog does not really become smaller!!
→ no real cost benefit for analog
Analog design versus scaling

- **Supply voltage drops**
  - limits signal range

- **Intrinsic gain drops**:
  \[ A_{int} = \frac{g_m}{g_{DS}} \]

ITRS

- Reliability due to material, process, and structural changes, and novel applications.

- TIDDR, SRH, PBTI, HCI, RTN in scaled and non-planar devices

- Increasing statistical variation of intrinsic failure mechanisms in scaled and non-planar devices

- 3-D interconnect failure mechanisms

- Reduced reliability margins drive need for improved understanding of reliability at circuit level

- Reliability of embedded electronics in extreme or critical environments (medical, automotive, etc.)
Importance of reliability

- guarantee product lifetime
  - e.g. safety-critical applications
  - in an increasingly unreliable context
    - technology process
    - environment
  - without huge overdesign

IC reliability

- spatial unreliability
  - manufacturing process variations
  - random defects
IC reliability

- **spatial unreliability**
  - manufacturing process variations
  - random defects

- **temporal unreliability**
  - aging effects
    - $\text{HCI, NBTI/PBTI, TDDB}$

- **dynamic unreliability**
  - workload dependence
  - temperature variations
  - EMC
Device aging effects

- Hot Carrier Degradation
- Time Dependent Dielectric Breakdown
- Bias Temperature Instability

→ circuit perf degrades with time:

\[ \Delta V_{TH} = A t^n \]

\[ A = f(V_{DS}, V_{GS}, T, L, W, ...) \]
The effect of CMOS scaling

> 65nm CMOS
- 'large' transistors
- some effects can be considered deterministic: NBTI, (PBTI), HCI
- some effects are statistical: TDDB, variability

< 65nm CMOS
- PBTI besides NBTI
- 'atomic' scale transistor
- everything becomes stochastic

[Maricau IEEE JETCAS 2011]
[Maricau DATE 2011]

What do we need for analog circuits?

- compact models for all important unreliability effects
  - include all important factors
    » e.g. W/L, Vgs, Vds, T, ...
  - include interaction effects
    » e.g. Vds-Vgs for HCI
  - cover a broad continuous range of values
    » e.g. Vgs = [0V ... 1.5V], W=[0.08μm-10μm]
  - model time-varying stress effects
    » e.g. Vgs(t)= VGS + sin(0.5,1e6)
Hot Carrier degradation

- **channel hot carrier**
  - a well known phenomenon (>25 years)
  - interface traps due to impact ionization near drain
  - dominant for nMOS in saturation
    - high $V_{DS}$
    - high $V_{GS}$
  - impact at device level
    - $\Delta V_{TH}$, $\Delta \beta$, $\Delta g_0$

$$\Delta N_{IT}(t) = C \exp(\alpha_1 V_{GS}) \exp(\alpha_2 V_{GS}) t^{0.45}$$

[INSESC Jan 2013 © G. Gielen, KU Leuven]

ESAT-MICAS model

- based on Reaction-Diffusion (RD) model
- includes all important transistor parameters ($V_{gs}, V_{ds}, L, T$)
- DC and AC voltage stress
- parameter set to be extracted for every process

<table>
<thead>
<tr>
<th>$\Delta V_{TH}$</th>
<th>$A [(V_{GS} - V_{TH})K_n (\frac{n_{ps}}{L} t)^{1/4}]^{3/2}$</th>
<th>$K_n$</th>
<th>$E_m$</th>
<th>$E_{sat}$</th>
<th>$E_{sat}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{ox}$</td>
<td>$(V_{GS} - V_{TH})$</td>
<td></td>
<td></td>
<td>$E_{sat}$</td>
<td>$L+(V_{GS} - V_{TH})$</td>
</tr>
<tr>
<td>$V_{DSAT}$</td>
<td>$E_{sat} L (V_{GS} - V_{TH})$</td>
<td></td>
<td>$E_{sat}$</td>
<td>$\frac{1}{\rho_{ps}}$</td>
<td>$\mu_{eff}$</td>
</tr>
<tr>
<td>$\mu_{eff}$</td>
<td>$\frac{1}{(V_{GS} - V_{TH})}$</td>
<td></td>
<td></td>
<td>$\rho_{ps}$</td>
<td>$\mu_{eff}$</td>
</tr>
</tbody>
</table>

A: 1.0E-2, $n_x$: 1.21, $E_0$ [V/m]: 0.71E8, $E_a$ [eV]: -0.06
$\phi_0$ [eV]: 3.7, $\lambda$ [nm]: 7.8E-9, $t$ [nm]: 45E-9
$\mu_0$ [cm$^2$/V.s]: 235, $\# [V^{-1}]$: 0.95, $k$ [J/K]: 1.38E-23

[Maricau ESREF 2008]
Negative Bias Temperature Instability

- recent phenomenon
- NBTI important for pMOS
  - [also PBTI for nMOS below 65 nm]
- traps due to electro-chemical reaction with SiH
- large $V_{GS}$
- temperature activated
- relaxation phenomenon
  - interface traps: permanent part
  - oxide traps: recoverable part
- impact at device level
  - $\Delta V_{TH}$, $\Delta \beta$, $\Delta g_o$

\[ \Delta N_{IT} = C \exp\left(\frac{V_G}{\alpha}\right) t^{0.18} \]
Bias Temperature Instability model

\[ R \approx \begin{cases} \frac{m}{l} (V_{C_{I,0}} + (V_{p_{\text{ref}}}' - V_{C_{I,0}}')) \log_{10} (\tau_{p}) - n_{p} \log_{10} (\tau_{p}) (V_{p_{\text{ref}}}' - V_{C_{I,0}}') \geq 0 \\ \frac{m}{l} (V_{C_{I,0}} + (V_{p_{\text{ref}}}' - V_{C_{I,0}}')) \log_{10} (\tau_{n}) - n_{n} \log_{10} (\tau_{n}) (V_{p_{\text{ref}}}' - V_{C_{I,0}}') < 0 \end{cases} \]

\[
\log(P) = \log(B_{p} V_{p_{\text{ref}}}') + \int_{0}^{t} \left( r^{-p} + n_{\text{leak}} \right) d \log(r)
\]

\[ R, P = f(V_{p_{\text{ref}}}') \text{ with } V_{p_{\text{ref}}}' = V_{p_{\text{ref}}} \]

\[ D = (R + P)(C_{T1} + C_{T2}) \]

\[ \tau_{p} = 5.5, \tau_{n} = 65, n_{p} = 0.5, n_{n} = 0.55, B_{p} = 1.25, p = 0.15, n_{\text{leak}} = 0.11, F_{s} = 2.45, \]

\[ F_{T1} = 1e^{-3}, F_{T2} = 2.88e^{-5} \]

[Maricau, ESSDERC 2012]

NBTI model verification

[Maricau, Electronics Letters 2010]
Transistor aging in sub-65nm CMOS

- **aging effects become worse, even with high-k**
  - EOT reduces
    - $E_{eff}$ increases
  - new materials (high-k)
    - PBTI
  - SiO₂ Interfacial Layer
    - NBTI, HC, TDDB remains

\[
\text{EOT}_{90\text{nm}} = t_{\text{SiO}_2} \\
\text{EOT}_{32\text{nm}} = t_{\text{IL}} + \frac{\varepsilon_{\text{SiO}_2}}{\varepsilon_{\text{HK}}} t_{\text{HK}}
\]

---

**Stochastic BTI model**

- individual charges can change $\Delta V_{TH}$
- Poisson distribution for number of trapped charges ($N=\text{mean number of traps}$)
- exponential distribution for the impact of an individual defect ($\eta=\text{average impact}$)
- $\Delta V_{TH}=f(V_{gs},T)$
- $\sigma(V_{TH})=f(1/(WL))$

\[
F_N(\Delta V_{TH}, \eta) = \sum_{n=1}^{\infty} \frac{e^{-N} N^n}{n!} \frac{1 - \Gamma(n, \Delta V_{TH}/\eta)}{(n-1)!}
\]

[Maricau DATE 2011]
**Time-Dependent Dielectric Breakdown**

- PMOS and NMOS
- Statistical phenomenon
- Gate current increases
- High $V_{GS}$
- Soft BD – $I_g$ noise
- Hard BD – $k\Omega$ gate resistance

**TDDB model**

- **Soft breakdown**
  - Example: 65nm technology
    - 1V gate stress
    - 10 year stress time
  - Time to SBD follows a Weibull distribution
    - $\eta_{SBD} = 1.2$
    - $\beta = -30$

$$F(t_{SBD}) = 1 - \exp\left(-\left(\frac{t_{SBD}}{\eta_{SBD}}\right)^\beta\right)$$

[Maricau DATE 2011]
Soft breakdown example

- Aging creates spread
  - 65nm technology (1.7nm tox)
  - 0.8V gate stress
  - PDF after 0,1,10 year stress time

[Maricau DATE 2011]

Contents

- Motivation
- Aging modeling
- Reliability simulation
- Reliability-aware or resilient design
- Conclusions
Commercial tools

- transistor reliability analysis:
  - RelXpert (now part of Cadence)
  - Mentor Graphics ELDO Reliability Simulator
  - Synopsys HSPICE MOSRA

The backbone of these tools is developed in the nineties and is no longer adequate!

Transistor model for aging

\[
\Delta V_{TH} = \frac{q(N_{it} + N_{ov})}{C_{ox}}
\]

\[
g_o = (1 + \beta \Delta V_{TH}) \lambda_0 I_{DS0}
\]

\[
\mu_{eff} = \frac{\mu_0}{(1 + \theta(V_{GS} - V_{TH})) (1 + \alpha \gamma \Delta V_{TH})}
\]

[Maricau TCAD2011 & DATE2011]
Deterministic reliability simulation

\[ \Delta V_{th} = \frac{q N_{th}}{C_m} \]
\[ g_m = (1 + \beta \Delta V_{th}) \mu / r_{th} \]
\[ \mu_{th} = \left( 1 + \sigma (V_{th} - V_{th}) \right) \left( 1 + \sigma \Delta V_{th} \right) \]

Example: LC-VCO

- **5 GHz and low phase noise**
  - high output swing
  - high LC-tank Q-factor
  - protective gate capacitors (DC-bias not shown)
  - UMC 90nm

\[ L_{phase} \{ \Delta \omega \} = 10 \log \left( \frac{2 F k T}{P_x} \right) \left[ 1 + \left( \frac{\omega_0}{2 Q \Delta \omega} \right)^2 \left( 1 + \frac{\Delta \omega / f}{\| \Delta \omega \|} \right) \right] \]
Nominal simulation

- AC simulation shows sudden $V_{out}$ degradation (due to $g_o$ degradation)
- no frequency degradation
- failure due to Hot Carrier damage

Variability awareness

- process variability introduces stress variability
- transistor aging + process variability = yield(t)

$$\sigma(V_{TH}) = (1 - \sigma(\Delta V_{TH}))\sigma(V_{TH_0})$$

$$\sigma(\mu) = \frac{\sigma(\Delta V_{TH})\beta \mu_0}{(1 + \beta(\Delta V_{TH})^2)}$$
Variability-aware reliability simulation

- factor space exploration
  - screening
  - linear model
  - detect interactions
  - regression
  - interactions
  - weakly nonlinear effects
- polynomial RSM
  \[ \vartheta_j = a_0 + \sum_{k=1}^{m} a_kx_k + \sum_{k=1}^{m} \sum_{l=k+1}^{m} a_{kl}x_kx_l + \sum_{k=1}^{m} a_{k0}x_k^2 \]
- residual analysis
  - error estimation

[Maricau TCAD 2010]

Example: VCO

[Maricau TCAD 2010]
### Variability-aware reliability simulation

<table>
<thead>
<tr>
<th>#factors/ #NRS</th>
<th>$\bar{\sigma}_{\text{rel}}$ [%]</th>
<th>$\sigma_{0,\text{rel}}$ [%]</th>
<th>$\bar{\sigma}_{\text{dec}}$ [%]</th>
<th>$\sigma_{0,\text{dec}}$ [%]</th>
<th>Analysis Time [min/sec]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5/19</td>
<td>0.04</td>
<td>0.57</td>
<td>0.85</td>
<td>13.9</td>
</tr>
<tr>
<td>2</td>
<td>14/43</td>
<td>0.41</td>
<td>1.44</td>
<td>1.10</td>
<td>2.80</td>
</tr>
<tr>
<td>3</td>
<td>15/53</td>
<td>0.29</td>
<td>0.25</td>
<td>0.46</td>
<td>0.28</td>
</tr>
<tr>
<td>4</td>
<td>27/95</td>
<td>0.10</td>
<td>0.11</td>
<td>0.26</td>
<td>1.80</td>
</tr>
<tr>
<td>5</td>
<td>35/121</td>
<td>0.14</td>
<td>1.30</td>
<td>1.01</td>
<td>3.90</td>
</tr>
<tr>
<td>6</td>
<td>20/361</td>
<td>0.01</td>
<td>0.26</td>
<td>0.26</td>
<td>2.00</td>
</tr>
<tr>
<td>7</td>
<td>141/333</td>
<td>0.12</td>
<td>0.08</td>
<td>1.10</td>
<td>4.00</td>
</tr>
</tbody>
</table>

1: One-stage Amplifier [Gain]
2: LC-VCO $[V_{osc}]$
3: Differential Pair Amplifier [Gain]
4: Symmetrical OTA [Offset]
5: Ring Oscillator [Frequency]
6: AND Gate [Fall Time]
7: IDAC [Normalized Output Voltage ($V_{out}/V_{ref}$)]

<table>
<thead>
<tr>
<th>$Y^* (t=0)$ [%]</th>
<th>$\bar{\sigma}_{\text{MC-RSM}}$ (t=0) [%]</th>
<th>Speedup</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>97.6</td>
<td>0.12</td>
</tr>
<tr>
<td>2</td>
<td>99.7</td>
<td>0.09</td>
</tr>
<tr>
<td>3</td>
<td>99.5</td>
<td>0.02</td>
</tr>
<tr>
<td>4</td>
<td>99.8</td>
<td>0.03</td>
</tr>
<tr>
<td>5</td>
<td>99.7</td>
<td>0.05</td>
</tr>
<tr>
<td>6</td>
<td>99.3</td>
<td>0.04</td>
</tr>
<tr>
<td>7</td>
<td>99.8</td>
<td>0.05</td>
</tr>
</tbody>
</table>

[Maricau TCAD 2010]

### Example circuit: ADC

[Gielen DATE 2013]
Impact on analog circuits

### Aging-insensitive analog circuits

- circuits that are immune to process variations
  - $\Delta V_{TH}<30\text{mV}@1\text{year}$
- examples:
  - oscillation frequency of an LC-VCO
  - passive feedback networks (e.g. active-RC filter)
  - gain, slew rate, bandwidth of an amplifier

$$H(s) = \frac{1}{s^2 + \frac{(R_1 + R_2)}{C_1 R_2} s + \frac{1}{R_1 R_2 C_1 C_2}}$$

[Maricau, ESSCIRC 2012]
Aging-sensitive analog circuits

- large operating voltages (i.e. \( V_{GS}, V_{DS} > V_{DD,nom} \))
  - e.g. phase noise of an LC-VCO

- asymmetrical stress can result in time-dependent mismatch
  - e.g. \( V_{offset} \) of a comparator

- time-dependent mismatch in matched transistors due to stochastic aging effects
  - e.g. MOS resistor in sub-45nm CMOS

Contents

- Motivation
- Aging modeling
- Reliability simulation
- Reliability-aware or resilient design
- Conclusions
Design for failure resilience

- **intrinsically robust circuits**
  - worst-case overdesign to account for P/V/T corners
  - plus overdesign to account for aging effects
  - consumes extra power and area

- **self-healing circuits**
  - adapt circuits at run time to compensate for the degradation
    - reconfiguration or retuning of the circuit
    - digital calibration
  - required performance is maintained, though degradation is present

- **fully redundant circuits**

Self-healing (sense & react) circuits

- **run-time monitoring and run-time adaptability**
  - add monitors or “canary” circuits to watch the degradation of the circuit performance
  - feed information to controller
  - real-time reconfigure circuit (e.g. extra components) or update circuit parameters (e.g. bias) to maintain the performance

for analog: this is compatible with evolution towards digitally-assisted analog
Example: high-voltage line driver

- output driver overview:

- equivalent model:

\[ \eta = \frac{P_{\text{load}}}{P_{\text{load}} + P_{\text{loss}}} = \frac{R_l}{R_l + R_{\text{on}}} \]

[Serneels ISSCC 2007]

- guarantee minimum power efficiency over lifetime
- breakdown monitors
- extra sub-transistors can be switched in

[De Wit DRVW 2008]
Self-healing test chip

- on-chip power efficiency monitor
  - measure output stage on-resistance ($R_{on}=2.25\Omega$)
  - compare current $R_{on}$ to reference resistor $R_{ref}$
- on-chip automatic controller
- chip measurements confirm real-time self-healing capabilities

Failure-resilient implementation

- 90nm CMOS technology
- $P_{load} = 10mW$, 90% efficiency
- modifications for failure-resilient operation: all included on chip!
Measurement results

- initial performance (fresh circuit): $\eta = 82\%$
- no reconfiguration: $\Delta \eta = 5.5\%$
- with reconfiguration: $\Delta \eta_{\text{max}} < 1\%$

[De Wit JSSC 2012]

Conclusions

- handling uncertainty, spatial and temporal reliability are a big issue in nanometer CMOS design
  - more degradation effects and becoming stochastic
- accurate modeling and efficient CAD tools are needed to assist the designer
  - support design for reliability
  - less need for guardbanding – lower design margins
- results have been proposed in this presentation
  - accurate transistor aging models for BTI, HCI and TDDB effects
  - efficient circuit reliability simulator methods
    - both nominal and stochastic effects
  - resilient design solutions with limited overhead
    - self-healing circuits through run-time adaptive sense&react principle
On-going PhD projects

✈ CAD :
  • reliability modeling and simulation
  • high-frequency circuit synthesis
  • automated analog behavioral modeling

✈ design :
  • ultra-low-power wireless sensor networks
  • autonomous sensor interfaces
  • imager readout circuits
  • biomedical interface circuits
  • digitally assisted analog
  • resilient self-healing analog circuits