Solid State Bipolar Marx Modulators:
Overvoltage Tolerance Capability

Hiren Canacsinh$^{1,2}$, Luís M. Redondo$^{2}$
$^{1}$INESC-ID, Lisboa
$^{2}$Instituto Superior de Engenharia de Lisboa, ISEL, GIAAPP
Lisboa, Portugal

J. Fernando Silva$^{1,3}$
$^{1}$INESC-ID, Lisboa
$^{3}$Instituto Superior Técnico, Universidade de Lisboa
Lisboa, Portugal

Abstract—Two solid-state bipolar Marx modulators are compared in terms of semiconductors overvoltage tolerance capability in abnormal operating conditions such as switching synchronization failure. Simulation results are presented for 4 stages of two Marx circuits using 500 V per stage with 1 kHz bipolar pulse repetition rate, with 5 µs pulse width and 10 µs relaxation time into resistive load.

I. INTRODUCTION

Through the years, power semiconductors increased their importance in pulsed power topologies named the Marx generator, conferring flexibility, higher pulse frequency and duty cycle, [1-5]. The increase of interest, for instance, from food and water purification industry applications for compact modulators and for bipolar pulses led to development of solid-state bipolar Marx modulators, [6-10]. However, in one hand topologies with additional switches for fault capability require complex triggering circuit on another hand optimized topologies, with reduced number of switches in each cell, uses some switches for more than one operating mode, contributing to the lack of current modularity of Marx type circuits, [11]. Aggravating this feature, the parallel charging technique increases the current in charging switches that are near the power supply [12]. Thus, when designing a solid-state Marx modulator, power semiconductors selection is also to be considered, not only by current rating but also by overvoltage across the switches in abnormal switching operation among operating modes.

The purpose of this paper is to present an analysis of semiconductors voltages in two solid-state bipolar Marx modulators presented in Fig. 1, under failure condition such as switch synchronism failure and open fault, considering that the semiconductors remain open-circuited when defective.

II. SEMICONDUCTORS VOLTAGE

Fig. 1 presents two solid-state bipolar Marx modulators, having each with $n$ stages, with IGBTs as on-off switches as described in detail elsewhere [8-9]. The main three operating modes of circuits of Fig. 1 are summarized in Table I. For clearness the IGBT anti-parallel diodes are not labelled in the circuits of Fig. 1, being named after the IGBT device number (e.g., $D_{a1}$ corresponds to the anti-parallel diode of IGBT $T_{a1}$).
TABLE I
SEMICONDUCTORS TURNED ON OF THE CIRCUITS OF FIG. 1 FOR CHARGING AND PULSE OPERATING MODES

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Operating mode</th>
<th>Charging</th>
<th>Positive Pulse</th>
<th>Negative Pulse</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fig. 1a)</td>
<td>Tₙ &amp; Tₐ or Tₙ &amp; Dₙ &amp; Tₐ or Tₙ &amp; Dₙ &amp; Tₐ</td>
<td>Tₙ &amp; Tₐ</td>
<td>Tₙ &amp; Tₐ</td>
<td>Tₙ &amp; Tₐ</td>
</tr>
<tr>
<td>Fig. 1b)</td>
<td>Tₙ &amp; Tₐ</td>
<td>Tₙ &amp; Tₐ</td>
<td>Tₙ &amp; Tₐ</td>
<td>Tₙ &amp; Tₐ</td>
</tr>
</tbody>
</table>

The solid-state bipolar Marx modulators presented in Fig. 1 and the switch path for charging and pulse operating modes shown in Table I are considered. Also, the collector to emitter switch ON voltage and anode-cathode voltage of ON diodes are considered to be approximately zero. The following sections will present an analysis of the switch voltages in the circuits of Fig. 1 under faulty condition such as switch synchronization failure (leading to brief open faults).

1) Charging the capacitors

Considering the circuit of Fig. 1a) and in case of synchronization failure (delay) of switch Tₙ or Tₐ of any independent (i) stage, the hold-off voltage across the delayed switch is the difference between voltages of capacitors Cᵢ and Cᵢ₊₁, Vᵢ₊₁ − Vᵢ. In case of failure of both Tₙ and Tₐ switches, these switches share the above voltage difference. In any of these individual or simultaneous switch failures, the set of switches Tᵢ and Tₐ share the voltage of Vᵢ or Vᵢ₊₁, respectively, as listed in Table II. Considering now the circuit of Fig. 1b), similar situation happens in case of individual or simultaneous failure of switches Tₙ and Tₐ, as shown in Table II.

2) Positive pulse

Considering circuit of Fig. 1a) in positive pulse operating mode, and considering delays in switches Tₙ or Tₐ, these switches hold-off the voltage of Vₐ in case of individual or simultaneous failure as listed in Table II. However, this is different for circuit of Fig. 1b), because the failure of switch Tₐ implies that this delayed switch has to sustain a voltage nearly equal two times the power supply voltage, i.e. 2Vₑₑ. Considering yet the circuit of Fig. 1b) and for situations of individual failure of switch Tₐ or simultaneous failure of switches Tₙ and Tₐ, the delayed switch(es) hold-off the Vₑₑ voltage, as shown in Table II.

TABLE II
FAULT CLEARANCE PATH AND HOLD-OFF VOLTAGE OF SEMICONDUCTORS FOR CHARGING AND PULSE OPERATING MODES OF THE CIRCUITS OF FIG. 1 AND THE OUTPUT VOLTAGE UNDER FAULT CONDITION

<table>
<thead>
<tr>
<th>Operat. mode</th>
<th>Circuit</th>
<th>Switch in fault condition</th>
<th>Hold-off voltage of faulty switches</th>
<th>Hold-off voltage of switches in OFF-state driven</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fig. 1a)</td>
<td>Tₙ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
</tr>
<tr>
<td></td>
<td>Tₐ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
</tr>
<tr>
<td>Fig. 1b)</td>
<td>Tₙ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
</tr>
<tr>
<td></td>
<td>Tₐ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
</tr>
<tr>
<td></td>
<td>T₉ &amp; Tₐ</td>
<td>Vₑₑ + Vₑₑ = Vₑₑ</td>
<td>Vₑₑ + Vₑₑ = Vₑₑ = 0</td>
<td>Vₑₑ + Vₑₑ = Vₑₑ = 0</td>
</tr>
<tr>
<td></td>
<td>Tₙ &amp; T₀</td>
<td>Vₑₑ = 2Vₑₑ</td>
<td>Vₑₑ = Vₑₑ = 0</td>
<td>Vₑₑ = Vₑₑ</td>
</tr>
<tr>
<td></td>
<td>Tₐ</td>
<td>Vₑₑ = 2Vₑₑ</td>
<td>Vₑₑ = Vₑₑ = 0</td>
<td>Vₑₑ = Vₑₑ</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Operat. mode</th>
<th>Circuit</th>
<th>Switch in fault condition</th>
<th>Hold-off voltage of faulty switches</th>
<th>Hold-off voltage of switches in OFF-state driven</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fig. 1a)</td>
<td>Tₙ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
</tr>
<tr>
<td></td>
<td>Tₐ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
</tr>
<tr>
<td>Fig. 1b)</td>
<td>Tₙ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
<td>Vₑₑ = Vₑₑ − Vₑₑ = 0</td>
</tr>
<tr>
<td></td>
<td>Tₐ</td>
<td>Vₑₑ = 2Vₑₑ</td>
<td>Vₑₑ = Vₑₑ = 0</td>
<td>Vₑₑ = Vₑₑ</td>
</tr>
<tr>
<td></td>
<td>T₉ &amp; Tₐ</td>
<td>Vₑₑ + Vₑₑ = Vₑₑ</td>
<td>Vₑₑ + Vₑₑ = Vₑₑ = 0</td>
<td>Vₑₑ + Vₑₑ = Vₑₑ = 0</td>
</tr>
</tbody>
</table>
3) Negative pulse

To apply negative pulse in circuit of Fig. 1a), switches $T_{ni}$ and $T_{hi}$ are turned ON. However, if any of these switches in each independent stage individually or simultaneously fails to turn ON the hold-off of voltage of faulty switch or switches is $V_{dc}$, as shown in Table II. This voltage condition is similar to the circuit of Fig. 1b) in case of failure switch $T_{ai}$ or simultaneous switches $T_{af}$ and $T_{bi}$, but is not verified in case of individual failure of switch $T_{di}$, as this switch has to hold-off the $V_{dc}$ voltage, as illustrated in Table II.

### III. SIMULATION RESULTS

The circuit of Fig. 1, with four stages was simulated in SIMULINK, MATLAB software. The simulated circuit was operated with $V_{dc} \approx 500$ V, 1 kHz, and 5 $\mu$s pulses width. The switch synchronism failure was simulated by delaying 1 $\mu$s to turn ON switches, $T_a$, $T_b$, $T_c$, and $T_d$ of the first stage in regard of other stages switches.

In Fig. 6 are shown the simulated results for switches: a) $T_{ai}$, $T_{bi}$, $T_{ci}$ and $T_{di}$, and b) $T_{ei}$ and $T_{fi}$, voltages, during normal charging and abnormal pulse (positive and negative) operating modes.

![Fig. 6 - Simulation results for the hold-off voltage of switches of the circuit of Fig. 1a) with lack of synchronism of simultaneous switches $T_{ai}$ and $T_{bi}$ for positive pulse and $T_{ei}$ and $T_{fi}$ for negative pulse: a) switches $T_{ai}$, $T_{bi}$, $T_{ci}$ and $T_{di}$ hold-off voltage and the output voltage; b) switches $T_{ei}$ and $T_{fi}$ hold-off voltage and the output voltage. The scales are 5 $\mu$s/div (horizontal) and 500 V/div (vertical).](image)

Considering Fig. 6a) and during charging operating mode, the set of switches $T_{ai}$ and $T_{bi}$ or $T_{ei}$ and $T_{fi}$ shares the voltage of $V_{dc}$. Considering pulse operating mode, and during the lapse of synchronism of switches $T_{ai}$ and $T_{bi}$ or $T_{ei}$ and $T_{fi}$ for positive and negative pulse, respectively, these switches hold-off the $V_{dc}$ voltage accordingly to section II. Regarding switches $T_{ei}$ and $T_{fi}$ (Fig. 6b)), during negative delayed condition, switch $T_{ei}$ holds-off the $V_{dc}$ voltage, but the voltage across switch $T_{fi}$ is approximately zero, because the anti-parallel diode $D_{ei}$ is forward biased. This is similar for switches $T_{ai}$ and $T_{bi}$ for abnormal positive pulse condition, as these switches hold-off a voltage of $V_{dc}$ and switch $T_{fi}$, but switch $T_{ei}$ voltage is zero, due to the anti-parallel diode $D_{ei}$ becomes forward biased.

Fig. 7 shows the simulated waveforms for hold-off voltage of switches $T_{ai}$, $T_{bi}$, $T_{ci}$ and $T_{di}$ during different operating modes and the output voltage of circuit of Fig. 1b). Considering charging period, switches in OFF-state ($T_{ai}$ and $T_{bi}$) hold-off a voltage of $V_{dc}$, as described in section II. In negative pulse operating mode and during synchronization failure of switch $T_{ai}$, this switch has to hold off the double ($2V_{dc}$) of the $V_{dc}$ voltage while the switches $T_{ai}$ and $T_{di}$, voltage is approximately zero because the anti-parallel diodes $D_{ai}$ and $D_{gi}$ are forward biased. This situation is analogous for switch $T_{ei}$ with respect of lack of synchronism during positive pulse operating mode, where the switch $T_{ei}$ has to hold-off the voltage of $2V_{dc}$ and the voltage across the OFF-state driven switches $T_{bi}$ and $T_{ei}$ is approximately zero, as can be seen in Fig. 7.

![Fig. 7 - Simulation results for the hold-off voltage of switches $T_{ai}$, $T_{bi}$, $T_{ci}$ and $T_{di}$ of the circuit of Fig. 1b) with lack of synchronism of switches $T_{ai}$ and $T_{bi}$ for positive pulse and negative pulse, respectively. The scales are 5 $\mu$s/div (horizontal) and 500 V/div (vertical).](image)

### IV. CONCLUSIONS

A comparative analysis of two solid-state Marx modulators was presented in terms of hold-voltage in abnormal switching operating condition such as switching synchronization failure.

Simulation results shows that in circuit of Fig. 1a) the maximum hold-off voltage of any switch within fault condition is $V_{dc}$ against the hold-voltage of $2V_{dc}$ for faulty switches $T_{ai}$ and $T_{ei}$ of circuit of Fig. 1b) for positive and negative operating mode, respectively, presenting a hold-off voltage asymmetry between semiconductors at the same stage.

### V. ACKNOWLEDGEMENTS

This work was supported by national funds through Fundação para a Ciência e a Tecnologia (FCT) with reference UID/CEC/50021/2013.
References


