Modeling of Power Supply Transients for EMI Compliance in Digital Systems

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Abstract

This paper addresses the modeling of power supply voltage transients in digital systems, in order to estimate the system's tolerance to this disturbance, in order to demonstrate EMI/EMC standard compliance. Electrical simulation is extensively used to demonstrate the possibility of exploiting the duality between time excitation and delay response, for combinational CUT (Circuit Under Test). We refer this as the "accordion" effect. The proposed technique makes use of concepts derived from the VLV (Very Low Voltage) testing and V_{DD} ramp testing techniques. Two regions of operation under ΔV_{DD} voltage drop are defined through the threshold power supply voltage, V_{DDth}, parameter. Electrical simulation supports the method, recently proposed, to perform fault simulation either by using faulty delays (defect size proportional to ΔV_{DD} magnitude) in the CUT and nominal time excitation rate, or by using a fault-free CUT description and faster test application times. Furthermore, for sequential circuits it is shown that the tolerance to ΔV_{DD} disturbances may be significantly lower than the one observed in combinational CUTs, due to de-synchronization effects in storage elements.

1. Introduction

Stringent requirements for advanced analogue, digital and mixed-signal chips include compliance to EMI/EMC standards [1]. One of the environmental disturbances that may occur is a transient power supply voltage, $V_{DD}(t)$, or power supply noise [2], which may induce circuit malfunction. For digital, malfunction can correspond to incorrect logic behavior, and/or incorrect system performance (timing failure). Products should be, as much as possible, *tolerant* to such transients, especially those for which the minimum V_{DD} value enables correct digital operation. This is relevant, not only for application-specific ICs, but also for reconfigurable devices, namely FPGAs [3]. In order to estimate the tolerance of the system, in the design phase, a procedure to model, inject and simulate such intermittent faults (IF) is required. Here, we consider that the *impact* of a physical defect or an environmental disturbance (causing a temporary modification) on system behavior and performance is modeled by an intermittent fault.

Cost-effective intermittent fault modeling, injection and simulation is not a trivial task. In fact, mature software tools target permanent faults (PF). Moreover, V_{DD} transients are accurately modeled at electrical level; however, digital fault simulation for complex modules needs to be performed, at least, at logic level. Recently, a novel methodology has been proposed [4], which aims at reusing PF simulation tools (commercial tools) for intermittent faults (IF) simulation, at logic level. In [4], the authors consider combinational circuits, a set of simplifying assumptions, and concentrate on describing a fault injection and simulation technique, using the PLI interface and the Verilog™ Cadence simulation tool. No effort was made to model the dependence of the delay *defect size* on the magnitude of the power supply voltage drop, ΔV_{DD}, nor to define at which levels of $V_{DD}(t)$ the transient can go until the functionality breaks down. In order to cause a system timing failure, the defect size of the delay fault must exceed the signal path slack. The *path slack* is defined as the difference between the time allowed for signal propagation (the clock period, τ_o) and the path length.

In this paper we focus on modeling power supply transients in digital modules (combinational and sequential). The goal is, using extensive electrical simulation (with SpectreS™, from Cadence), to identify the major factors contributing to ΔV_{DD} transient's tolerance, and to characterize their effects at logic level, as dynamic faults, through delay modulation.

The paper is organized as follows. In section 2, previous work on the topic is reviewed. Section 3 describes the proposed methodology. Simulation results for combinational, synchronized and sequential circuits are presented in section 4. Finally, section 5 summarizes the main conclusions of the work.

2. Previous Work

The power supply voltage, V_{DD}, is a variable absent from the *logic level* modeling and simulation environment. Assumed as constant (nominal value), it contributes to the definition of analog voltage domains for which Boolean values, '0' or '1', can be identified. Data processing manipulates Boolean algebra, and the power supply voltage plays a role similar to the substrate (or well) regions in the semiconductor device: they must to be there, be biased, but they are assumed to be latent, just enabling the electrical isolation associated with the reverse biasing of the p-n junctions. Similarly, the V_{DD} voltage source must be there, exhibit a constant value and provide the power the circuit needs to perform its function. However, the *exact* (and maybe not so latent) value of V_{DD} has a strong influence on the circuit's speed response. Especially for high-speed products, for which the clock rate is pushed to the limit allowed by the manufacturing technology and process variations, the role of V_{DD} on system performance deserves attention. This is more even so, when emerging nanometer technologies become mainstream technologies and digital circuits behave more like analog circuits.

In order to apply a high-quality test in the manufacturing line, researchers have extended their work on permanent faults from *static* to *dynamic* faults. *Delay fault testing* has emerged [5], and a significant work has been carried out since then (see, e.g., [6], [7] [8], [8], [9], [10], [11], [12]). Factors affecting the timing characteristics of a given system, such as process variations, manufacturing defects, noise and other environmental disturbances, are often statistical in nature; hence, statistical approaches have also been under scrutiny [13] [14]. In such context, the goal is to *uncover* dynamic faults, thus implying that high-quality, robust delay tests need to be generated. Our goal is the opposite: we want the IC to be *tolerant* to dynamic faults, either permanent, or intermittent, such as ΔV_{DD} disturbances, under investigation. Nevertheless, all the techniques derived so far to *detect* dynamic faults can be of interest to define a strategy for modeling, injecting and simulating ΔV_{DD} faults.

The power supply voltage variable has been used in the context of increasing the test and diagnostic capabilities for digital, analog and mixed-signal systems. For digital, some physical defects, undetectable with nominal V_{DD} values, can be uncovered by VLV (Very Low Voltage) testing [15]. VLV testing is a test method that operates a CUT (Circuit Under Test) at reduced V_{DD} voltage *and speed* to detect functional (Boolean), timing or power supply current (I_{DDQ}) failures. For instance, lowering V_{DD} eases the detection of resistive bridging defects, as with VLV testing the pull-up/pull-down MOSFET on-resistances significantly increase with lower V_{DD} [16]. The detection of delay faults also can be enhanced by VLV test [17]. For analog circuits, it has been observed that, by ramping up the V_{DD} supply voltage, the MOSFET transistors undergo through all regions of operation, which significantly increase the diagnostic resolution, namely using the power supply current signature. Hence, a methodology has been proposed in the 90's [18], and recently extended to test RF circuits [19].

The awareness that V_{DD} significantly can influence the system's performance has also been used to enhance test effectiveness, in additional ways. The effectiveness of a vector pair to uncover a path delay fault strongly depends on the path's propagation delay and the defect size. Critical paths exhibit the smaller path slacks, while other path delay faults may remain undetected due to large path slacks [20]. Hence, a good method is to speed-up the test application time to offset delay fault coverage losses due to large slack paths [21] [22]. More recently, a multiple-clock scheme to enhance the effectiveness to uncover delay faults has also been proposed [23]. In such research work, however, nominal V_{DD} is used.

3. Methodology

A transient power supply voltage disturbance, $V_{DD}(t)$, basically can induce a functional failure (incorrect logic behavior), a timing failure (correct logic behavior, but not within the specified time frame), or both. In order to study the *tolerance* of the product to a ΔV_{DD} drop, the methodology proposed in this paper uses (1) the duality between ΔV_{DD} and $\Delta\tau$ (the abnormal delay of the CUT to produce a correct behavior), and (2) the knowledge gathered with the VLV testing and V_{DD} ramp testing techniques. The underlying methodology proposed in [4] is used. For combinational CUTs, it has been shown that the *time excitation – delay response duality* can be exploited. In fact, for combinational modules (or for the combinational parts of scan-based sequential circuits), to have a logic circuit that takes longer to respond (due to a

transient ΔV_{DD}) is equivalent to have a nominal circuit (without abnormal delays) and a test pattern applied (and CUT responses observed) at a higher clock frequency. If a V_{DD} ramp test is applied, an "*accordion*"-like effect becomes visible, as the CUT response progressively slows down with V_{DD}. Two fault injection techniques have been used (1) nominal clock and observation rates, and CUT with abnormal (larger) delays in all logic elements; (2) fault-free CUT, abnormal (faster) clock and observation rates. The first technique requires fault injection by modification of the delays stored in the cell library, through the PLI interface of the Verilog™ tool; the second technique, using the fault-free CUT, requires significantly less computational effort than the first technique.

In order to use logic-level ΔV_{DD} drop fault simulation, we need to validate the assumptions made in [4]. This is one of the major goals of this paper. The second goal is analyze what happens with storage elements, and sequential circuits. The next sections report the results obtained with low-level, electric simulation.

Consider the disturbance associated with a $V_{DD}(t)$ transient. This transient is characterized by two parameters: ΔV_{DD} (pulse magnitude), and Δt (pulse width). These parameters are never known a priori, so a statistical distribution may be assumed.

The impact of the **V_{DD} pulse magnitude** on CUT response can be described in two regions:

- **Region I** - For limited ΔV_{DD}, functionality holds, but performance tends to be reduced. If it is reduced within the margin tolerated by the path slack, performance holds according to specifications. Otherwise, a timing failure will occur.
- **Region II** - For large ΔV_{DD}, MOS transistors become unable to act as electronic switches, and functionality collapses. The exact value of the maximum ΔV_{DD} for which functionality holds depends on the CUT's topology and on its physical structure (circuit and layout level). Nevertheless, it is to be expected that, in combinational CUTs, the minimum value $V_{DD} - \Delta V_{DDmax} = V_{DDmin}$ that sustains the functionality (at lower speed) should be somewhere between $V_{DD}/2$ and.$(V_{tn} + |V_{tp}|)$ [17]. We refer $V_{DDmin} = \mathbf{V_{DDth}}$ as the *threshold power supply voltage*, which separates Regions I and II. In [3], using a V_{DD}=5 V, for V_{DD} values "substantially bellow 3 V", FPGA configuration and data hold, while "V_{DD} dips bellow 2.3 V" might corrupt the stored configuration.

V_{DD} pulse width also impacts CUT response. For *fast* transients ($\Delta t << \tau_{oNOM}$), it is expected that both functionality and performance will hold. For typically *slow* transients ($\Delta t >> \tau_{oNOM}$) and Region I ΔV_{DD}, functionality will hold, but performance may not hold.

4. Simulation Results

4.1 Combinational Modules

First, a detailed analysis of circuit performance under $V_{DD}(t)$ transients has been performed, using electrical simulation on simple combinational logic: 7 inverters (simulating a short signal path), 77 inverters (long path) and a ring oscillator. Impact of $V_{DD}(t)$ transient (of variable magnitude and duration) on voltage, delay and power supply current, $i_{DD}(t)$ has also been studied. In all experiments, Cadence EDA system is used, together with an AMS 0.35 μm CMOS design kit. Library cells were designed, using this technology, as no information on actual layout is available.

As shown in Figure 1, for this technology a slow ΔV_{DD} transient disrupts functionality for around $V_{DD}(t)$ = 1.0 V (V_{tn}=0.466 V and $|V_{tp}|$=0.617 V). As expected, for a combinational CUT, functionality is recovered as soon as the power supply voltage ramps up above this threshold value. For a 77 ring oscillator, the "accordion" effect is clearly visible (Figure 2) for $V_{DD}(t) > V_{DDth}$ (Region I). These results show that for combinational CUT, the threshold power supply voltage, V_{DDth}, is significantly low, i.e., close to .$(V_{tn} + |V_{tp}|)$. The effective tolerance of a CUT to this disturbance (the CUT uncovering a delayed response) depends on the specified time slack: the more you push performance, the less tolerance you get.

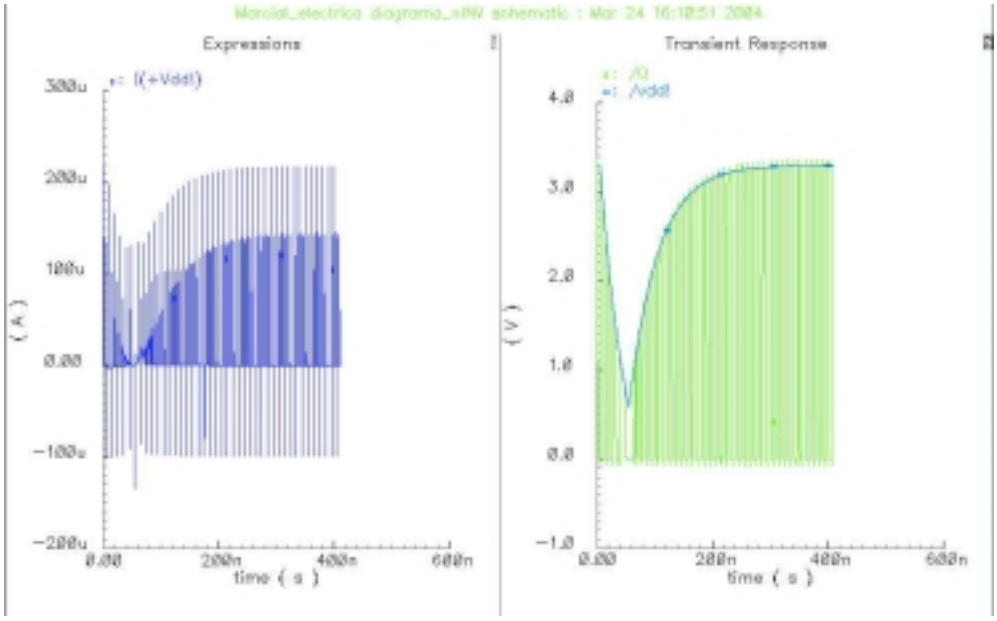

Figure 1 – Seven inverters chain transient response (power supply current, i_{DD}, and output voltage), τ_{oNOM}=10 ns, slow and deep V_{DD} transient ($\Delta t >> \tau_{oNOM}$, ΔV_{DD}=2.7V, V_{DD}=3.3 V).

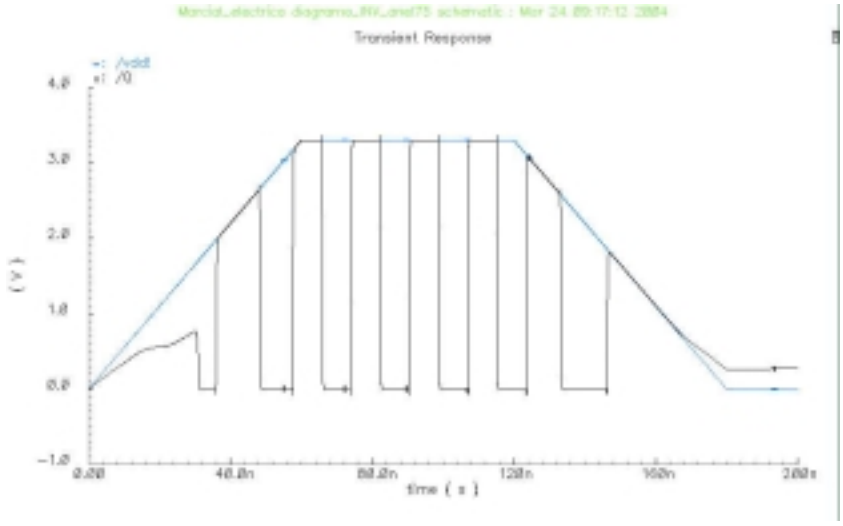

Figure 2 - Ring oscillator (77 inverters) transient response (power supply and output voltages), τ_{oNOM}=10 ns, V_{DD} power up and down fast transient ($\Delta t >> \tau_{oNOM}$, $\Delta V_{DD}=V_{DD}$, V_{DD}=3.3 V).

4.2 Synchronized Modules

For CUT with storage elements, operating in Region I under a ΔV_{DD} disturbance, a the single cause (increased delay of circuit elements, due to ΔV_{DD} drop) may induce two effects: (1) a timing failure directly resulting from the "accordion" effect – abnormal combinational path delay, exceeding the path slack, and/or (2) a timing failure due to a de-synchronization between the time slot in which correct Boolean values are available at the output of the combinational path, and the time slot in which the storage element captures the value at the path's output. In our experiments, we used a level-sensitive D-type Flip-Flop (FF). The effect to occurs first induces a timing failure, thus limiting the fault tolerance of the CUT to ΔV_{DD} transients.

This can be seen in the experiments performed with a 77 inverter chain terminated by a D-FF. Nominal V_{DD} = 3.3 V and ramp V_{DD} have been used. The V_{DD} ramp-up is characterized by a 1 ns power on (from 0

to 3.3 V), a 50 ns period at the nominal value (3.3 V) and 500 ns (slow) V_{DD} fall. The input signal has a τ_{oNOM} = 8 ns period, while the clock (CLK) has a 4 ns period; both exhibit a 50% duty cycle, and start at 3.3 V. An initial delay of 2 ns (case I, Figure 3, Figure 4) and 3.2 ns (case II, Figure 5, Figure 6) is applied to CLK, to synchronize the chain output and the clock signal. Input and CLK are fed to the CUT through a pair of inverters, so the typical (V_{DD} dependent) waveforms are applied to the CUT.

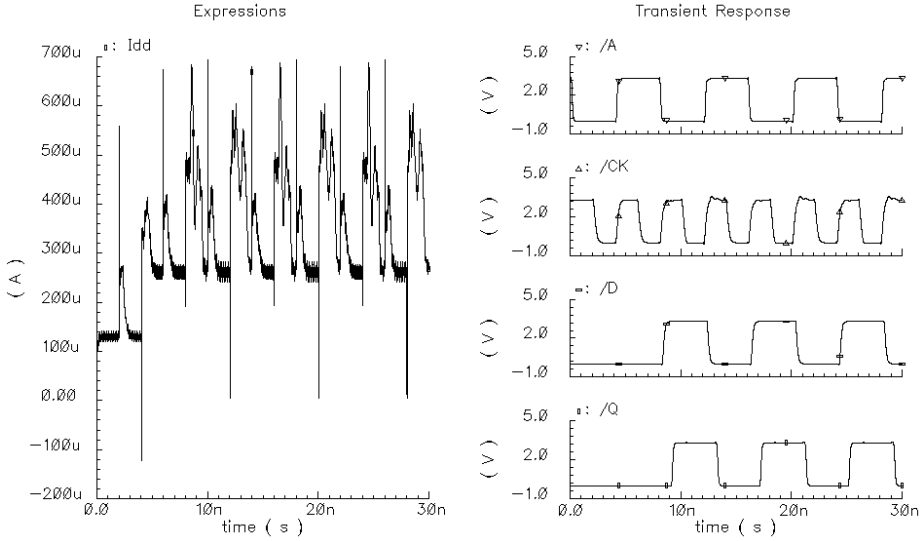

Figure 3 – Fault-free operation of the 77 inverter chain + D-FF (V_{DD} = 3.3 V) (case I)

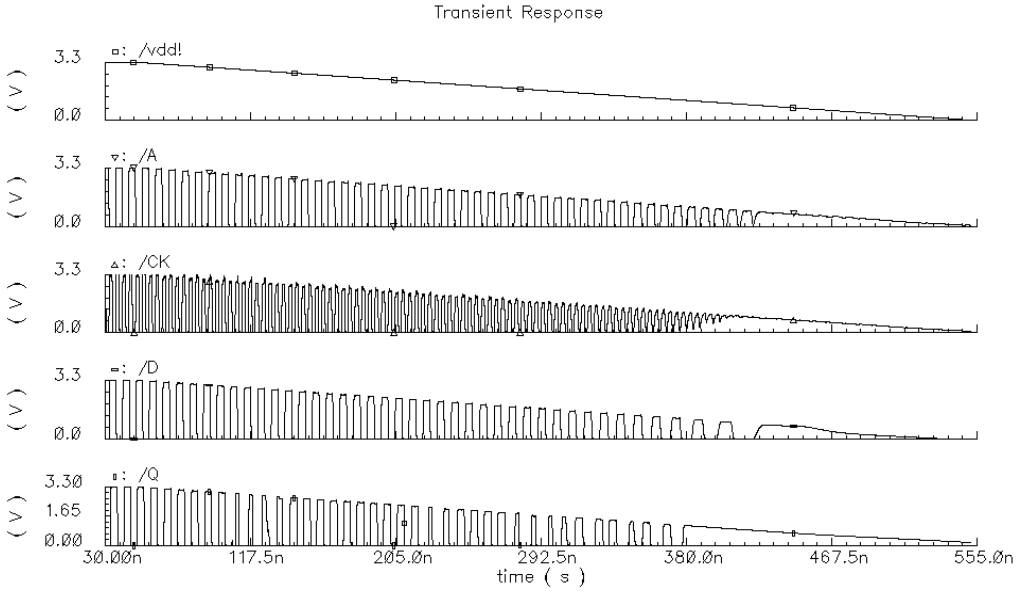

Figure 4 - 77 inverter chain + D-FF (V_{DD} fall) (case I). De-synchronization and "accordion" effects are shown

As it can be seen in Figure 3, in case I the D-FF captures the D signal at the beginning of the D pulse, while, in case II, the D-FF captures the D signal in the middle of the D pulse (Figure 5). Hence, with the same clock period, we change the capturing moment, which is relevant since, in the presence of the ΔV_{DD} disturbance, the D pulse is delayed according to the ΔV_{DD} drop magnitude. Case I leads to lower tolerance than case II. In fact, for case I (Figure 4), the first timing failure occurs, due to de-synchronization, at t=105 ns, for V_{DDth}=2.95 V (just 10.6% voltage drop). For case II (Figure 6), the first timing failure occurs, due to de-synchronization, at t=155 ns, for V_{DDth}=2.6 V (21.1% voltage drop). In all cases, the clock signal, fed through the inverters, decreases in amplitude, so that, for t=374.6 ns (and V_{DD}=1.17 V) the FF becomes unable to capture the D signal. These results show that, using a level-sensitive D-FF, the

second effect (de-synchronization) limits first the CUT tolerance to ΔV_{DD} than the first effect ("accordion" effect, associated with excessive delay in the combinational path).

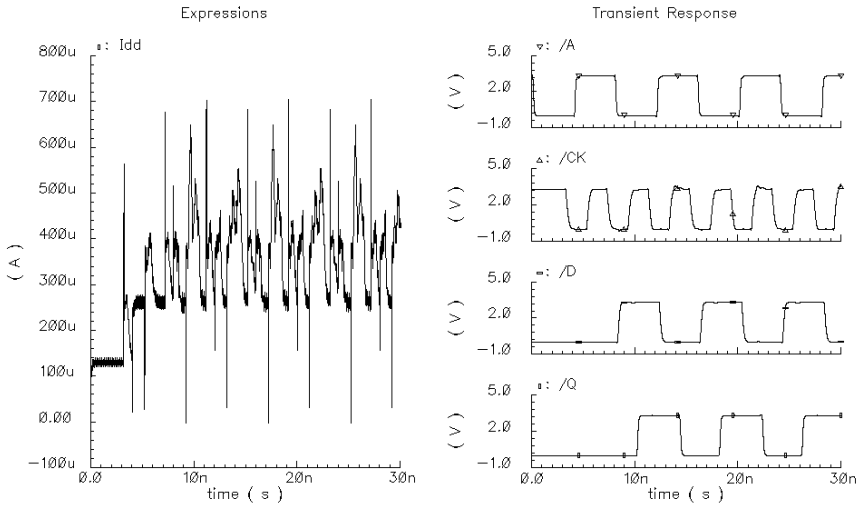

Figure 5 – Fault-free operation of the 77 inverter chain + D-FF (V_{DD} = 3.3 V) (case II)

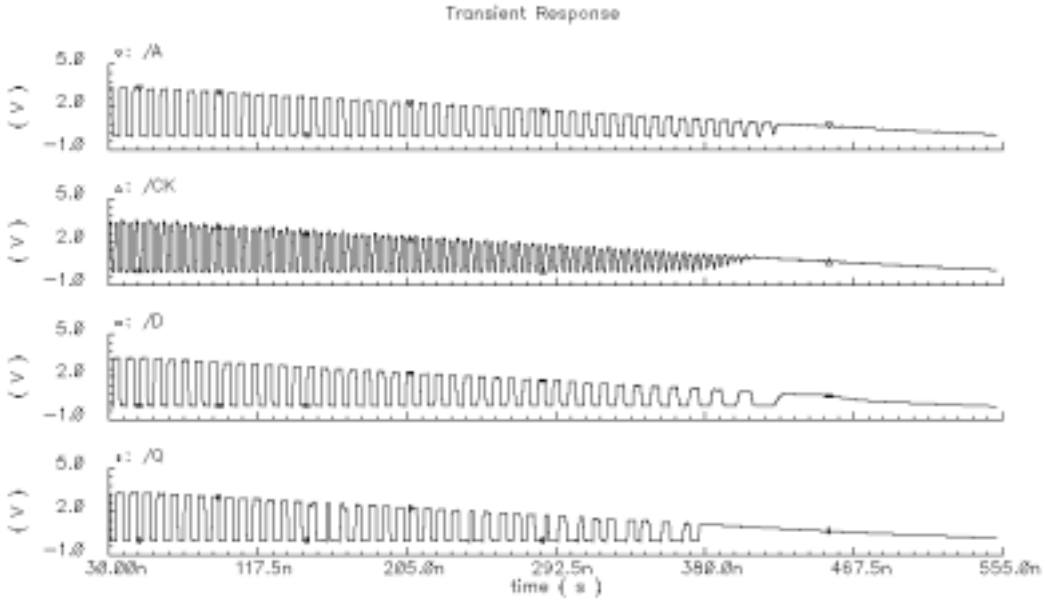

Figure 6 - 77 inverter chain + D-FF (V_{DD} fall) (case II).

4.3 Sequential Modules

A simple sequential module (the ISCAS'89 s27 benchmark circuit [24]) has been used to analyze the tolerance of a sequential CUT to ΔV_{DD} disturbances. The circuit (Figure 7) has 4 PI (Primary Inputs), 1 PO (Primary Output), 3 state variables (3 D-FFs feeding the 3 SO (Secondary Outputs) as 3 SI (Secondary Inputs)).. The only PO depends, in this case study, of all PI and SI, and is the complementary value of one of the SO (E_{1in}). Hence, we observe the SO (E_{2in}, E_{1in}, E_{0in}) and the SI (E_{2out}, E_{1out}, E_{0out}), looking for timing failures, in the presence of the V_{DD} ramp testing. The set of PI vectors is shown in Figure 8, traversing all states and allowing the activation of different signal paths in the combinational network. The clock signal has a 3.75 ns phase delay, and a 250 MHz frequency. The loop in PI values allows to easily following the CUT's responses, as V_{DD} slowly falls down. Note that, now, at the SO, we can spot the effect both of the delayed response of the combinational network *and* the de-synchronization effect due to unreliable SI applied at the combinational block at previous clock cycles.

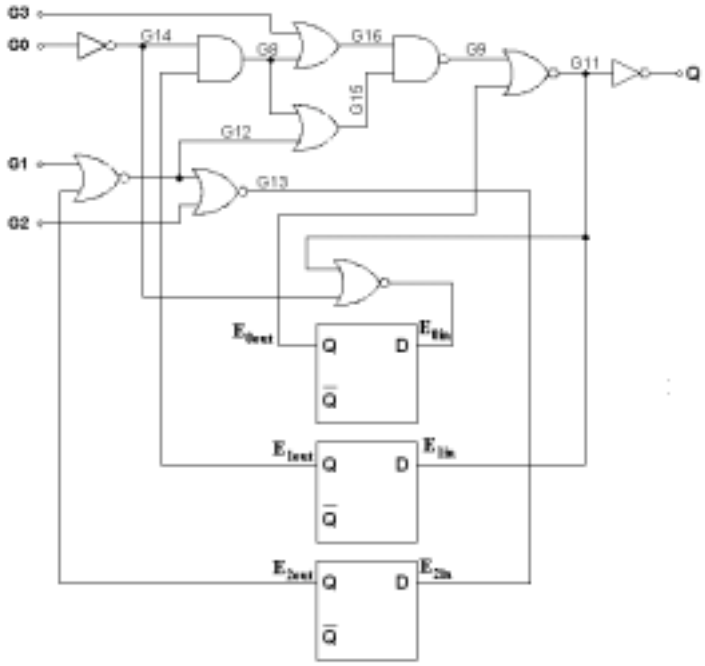

Figure 7 – s27 circuit diagram

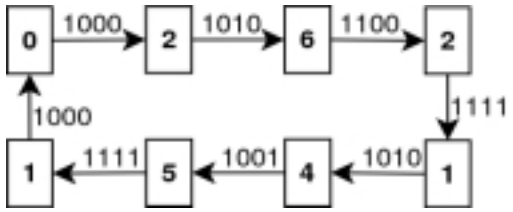

Figure 8 Test vectors applied (in loop) to the s27 CUT and reached states (G_3=1)

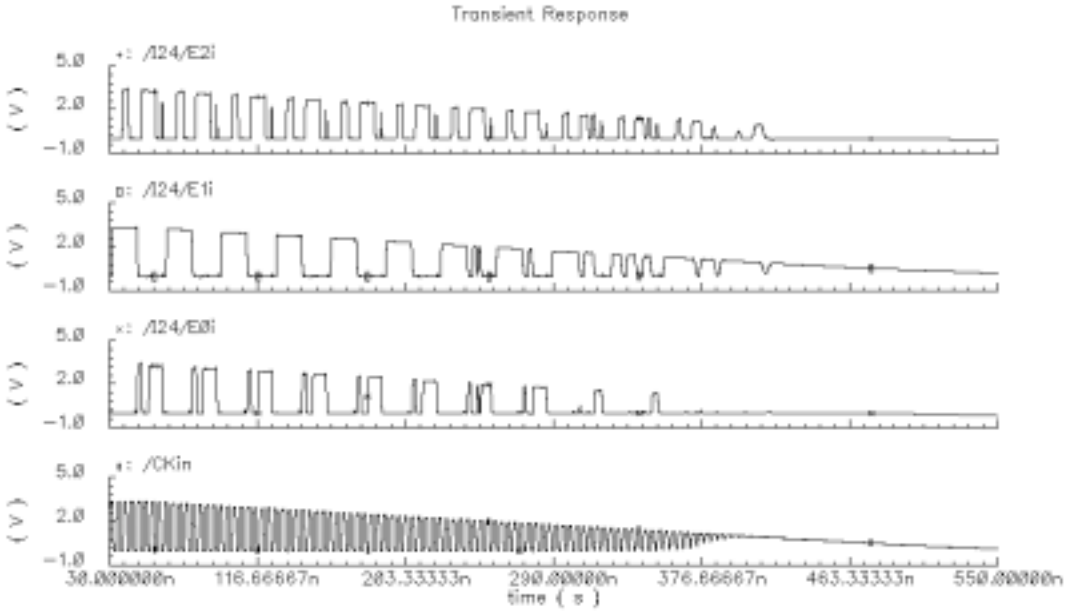

Figure 9 – s27 response (V_{DD} fall) (SO)

As it can be seen in Figure 9, a timing failure becomes visible at the PO (or at the E_{1in} SO) for t=250 ns, and with a threshold power supply voltage of V_{DDth}=1.99 V (39.7% voltage drop).

5. Conclusions

This paper addressed the modeling of power supply voltage transients in digital systems, in order to estimate the system's tolerance to this disturbance, in order to demonstrate EMI/EMC standard compliance. Tolerance may consider two levels: functional and timing. We considered the most constraining one, which is the one that leads to the definitions of domains for which the CUT performs its correct functionality and within the pre-specified time frame.

Electrical simulation was extensively used to analyze the behavior of combinational, synchronized (i.e., combinational blocks terminated by synchronizing registers) and sequential circuits under ΔV_{DD} voltage disturbances. The proposed technique makes use of concepts derived from the VLV (Very Low Voltage) testing and V_{DD} ramp testing techniques. We showed that ΔV_{DD} pulse *magnitude* and *width* influence the CUT's tolerance to this disturbance. Fast $V_{DD}(t)$ pulses (as compared to the clock period) typically do not disturb significantly the CUT's functionality (Boolean logic values) and performance (I/O propagation delay). *Slow* $V_{DD}(t)$ pulses are thus of interest, and we concentrate on ΔV_{DD} magnitude. Two regions of operation under ΔV_{DD} voltage drop have been defined; the frontier between them has been characterized through the threshold power supply voltage, V_{DDth}, parameter. Region I is the interesting region for disturbance tolerance evaluation. The key aspect that needs to be represented, at logic level, is the delay modulation. For each CUT, the estimation of V_{DDth} becomes relevant to define the domain of validity of the logic level delay fault model.

For combinational CUT, it was shown that it is possible to exploit the duality between time excitation and delay response. The "accordion" effect (delayed output response) defines the value of V_{DDth}. We showed that, this value is very low, typically in the order of $(V_{tn} + |V_{tp}|)$ (in the AMS 0.35 um technology, ΔV_{DD} voltage drop can reach 66%).

However, for synchronized and for sequential CUTs, a second effect becomes relevant, and may be even become the most constraining one: the timing failure due to de-synchronization between the (delayed) response of the CUT's combinational paths and the data capturing by storage elements. In our experiments, significantly higher values of V_{DDth} have been obtained (ΔV_{DD} voltage drops of 39.7% to10.6%).

Several factors limit V_{DDth} and the tolerance to ΔV_{DD}: semiconductor technology, CUT topology, type of storage elements (at present, edge-triggered D-FF are been tested), critical path delay as compared to storage element's delays, etc.. Future work includes the definition of a model to compute V_{DDth}, and of a model to estimate the dependence of the delay defect size on ΔV_{DD}. Moreover, a logic-level accurate model to describe abnormal delays (or to modulate the faster test application time) will be carried out.

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