Positive Realization of Reduced RLCM Nets

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***Abstract*—Model Order Reduction is nowadays routinely applied as a basic step in order to enable the efficient simulation of very large RLC linear models, such as extracted parasitics and circuit oriented EM extraction. Often, such reduced models are synthetized as a subcircuit and ported to simulation environments for multiple subsequent runs. Such an approach is quite common as often designers prefer to work with circuit netlists as opposed to abstract mathematical representations and furthermore, many simulators can only handle circuit elements. However, the potential advantages provided by the reduction may be compromised when the dense reduced models are synthetized to netlists due to the presence of non-physical elements (such as negative RLC) or a large number of controlled sources. Such issues may hinder efficiency or even completely preclude analysis as many simulators cannot handle non-physical elements whose handling is altogether questionable. This paper proposes a methodology for the synthesis of reduced order models of general multiport RLC nets amenable to be included in standard simulation environments. Unlike other previously published approaches, the methodology generates very compact models while guaranteeing the positiveness of the RLC values, which allows their direct confinement in any SPICE-like circuit simulator.**

I. Introduction

As VLSI circuit speeds and density continue to increase, design of modern high-performance electronic systems such as RF circuits, optical transceiver ICs, dense digital signal processing or data computation elements has become increasingly complicated. Not only has complexity risen, but increasing speed and density tend to exacerbate undesirable effects such as signal integrity problems and excessive electromagnetic interference or coupling, and therefore careful attention to physical modeling is required. To address these problems designers are faced with conflicting requirements: on one hand they want to extract and build complex models accounting for all relevant coupling and electro-magnetic effects; on the other hand they want the resulting model to be efficiently simulated/evaluated. Model order reduction (MOR) algorithms are now a standard procedure for obtaining simple models of complicated physical systems enabling designers to start from detailed level descriptions of coupling phenomena and return compressed, affordably simulated models. The effectiveness of MOR algorithms is judged by the decrease in final circuit simulation time, compared to simulation with the full model, assuming acceptable error is incurred in the modeling process.

Over more than a decade, MOR algorithms [1], [2] have been receiving significant attention, and while considerable research has been devoted to improving compactness and accuracy, much less attention has been devoted to the issue of how these models are used in analysis and simulation environments. Often, the mathematical representations output by MOR algorithms are directly input to simulators. However such an approach is not universal as many commercial environments do not allow such representations. Sometimes the reduced models are synthetized as a subcircuit and ported to simulation environments for multiple subsequent runs. Such an approach is quite common as often designers prefer to work with circuit netlists as opposed to abstract mathematical representations and furthermore, many simulators can only handle circuit elements. However, the potential advantages provided by the reduction may be compromised when the dense reduced models are synthetized to netlists due to the presence of non-physical elements (such as negative RLC) or a large number of controlled sources. Such issues may hinder efficiency or even completely preclude analysis as many simulators cannot handle non-physical elements whose handling is altogether questionable. In this paper we propose a new methodology for the synthesis of reduced order models of general multiport RLC nets amenable to be included in standard simulation environments. Unlike previously published approaches, the method generates very compact models while guaranteeing the positiveness of the RLC values, which allows their direct confinement in any SPICE-like circuit simulator.

This paper is structured as follows: in Section II basic model formulation and representation descriptions are discussed and compared. In Section III several realization techniques are discussed in order to generate a full-fledged electrical network whose behavior mimics that of the reduced model. In Section IV a new methodology is proposed for the synthesis of reduced order models of general multiport RLC nets amenable to be included in standard simulation environments. In Section V examples are shown that illustrate the efficiency and correctness of the proposed technique, and in Section VI conclusions are drawn.

II. Background and Problem Definition

A. Formulation and System Representation

In the general case of RLC circuits, the Modified Nodal Analysis (MNA) formulation provides a system representation of the netlist as a set of equations that form the time-domain state space representation [1]. This state space relates the inputs $u(t)$ to the outputs $y(t)$ via the defined inner states $x(t)$, i.e. the node voltages v and the currents i flowing through the branches with inductances or sources,

$$\begin{bmatrix} \mathcal{C} & 0 \\ 0 & \mathcal{L} \end{bmatrix} \begin{bmatrix} \dot{v}(t) \\ \dot{i}(t) \end{bmatrix} + \begin{bmatrix} \mathcal{G} & F_l^T \\ -F_l & 0 \end{bmatrix} \begin{bmatrix} v(t) \\ i(t) \end{bmatrix} = \begin{bmatrix} \mathcal{B} \\ 0 \end{bmatrix} u(t),$$
$$y(t) = \begin{bmatrix} \mathcal{B}^T & 0 \end{bmatrix} x(t), \tag{1}$$

where $\mathcal{G}$ is the matrix of stamped conductances, $\mathcal{C}$ is the matrix of stamped capacitances and $\mathcal{L}$ is the matrix of inductances,

and F_l is the inductance adjacency matrix that determine each inductance nodes. $\mathcal{B}$ is the incidence matrix that relates the ports to the inner states $x(t)$, a vector containing the voltages v and currents i. The (complex) frequency response can be obtained from the Laplace transform of (1), which is a system representation of a unique transfer function.

$$\begin{gathered}(sC+G)\,x(s)=Bu(s),\quad y(s)=Bx(s),\\ H(s)=B^T\,(sC+G)^{-1}\,B.\end{gathered} \tag{2}$$

where $C \in \mathbb{R}^{n\times n}$ is the dynamic system matrix, $G \in \mathbb{R}^{n\times n}$ is the static system matrix, and $\mathcal{B} \in \mathbb{R}^{n\times m}$ is the I/O matrix that relates the m ports to the inner states, $x \in \mathbb{C}^n$, and $H \in \mathbb{C}^{m\times m}$ is the frequency domain transfer function. Sometimes, the models resulting from the extraction are represented as a second order state space matrix descriptor

$$\begin{gathered}s\mathcal{C}x(s)+\mathcal{G}x(s)+\tfrac{1}{s}\mathcal{K}x(s)=\mathcal{B}u(s),\quad y(s)=\mathcal{B}^Tx(s),\\ H(s)=\mathcal{B}^T\left(s\mathcal{C}+\mathcal{G}+\tfrac{1}{s}\mathcal{K}\right)^{-1}\mathcal{B},\end{gathered} \tag{3}$$

where $\mathcal{K} = F_l^T\mathcal{L}^{-1}F_l$ is the susceptance (or K-elements, inverse of the inductances) matrix. The states in this case are solely the voltage on the nodes plus the currents flowing through the sources. There is a direct relation between the first (1) and second order (3) state space representations, but the straightforward transformation from one to another requires the inversion of $\mathcal{L}$, which may be expensive.

B. Model Order Reduction and Projection

For a complete analysis, a linear system of dimension n has to be solved. Thus when the size of the system is large, the analysis of the function in (2) becomes prohibitive. To overcome this issue, Model Order Reduction (MOR) approaches seek to efficiently generate an accurate approximation of order $q \ll n$, which faithfully approximates the original behavior.

The most common procedure to obtain an accurate and structurally similar Reduced Order Model (ROM) is to use an orthogonal projection on the matrix representation [1], [2]. Standard MOR methodologies rely on the generation of a suitable low order subspace (spanned by the basis $V \in \mathbb{R}^{n\times q}$), in which the original system matrices C, G, and B are projected, via a congruence transformation. This generates a ROM with an associated transfer function $\widehat{H}(s)$,

$$\begin{gathered}\widehat{C}\dot{\widehat{x}}(t)+\widehat{G}\widehat{x}(t)=\widehat{B}u(t),\quad y(t)=\widehat{B}^T\widehat{x}(t),\\ \widehat{H}(s)=\widehat{B}^T\left(s\widehat{C}+\widehat{G}\right)^{-1}\widehat{B}\approx H(s),\end{gathered} \tag{4}$$

where $\widehat{C} = V^TCV$, $\widehat{G} = V^TGV$ are $\mathbb{R}^{q\times q}$ matrices, $\widehat{B} = V^TB$ is a $\mathbb{R}^{q\times m}$ matrix, and $\widehat{x} \in \mathbb{R}^q$ is the reduced set of states, of dimension $q \ll n$. The congruence projection has a key advantage: it preserves the system passivity under certain structural properties, and these properties are fulfilled by the MNA formulation (see [1] for details). Despite the advantages of the projection based reduction, the ROMs so generated have some inherent drawbacks. One of the most relevant is that the original inner structure of the matrices is lost after the reduction, and the reduced matrices are full, which may have consequences in the ROM usage, as we shall see.

To palliate these issues, block structure preservation (BSP) schemes have been proposed, which allow to maintain a desired block structure, and some block sparsity [3]. If the system matrices exhibit block structure the subspace projector V can be split and restructured into a block diagonal one so that the block-level structure is preserved under congruence transformation. For instance considering the structure from (1),

$$V=\begin{bmatrix}V_1\\ V_2\end{bmatrix}\rightarrow\begin{bmatrix}V_1 & \\ & V_2\end{bmatrix}=\bar{V} \tag{5}$$

After projection, the the inherent variable structure of the MNA formulation (1) is kept, which will enable, as we shall see, to re-interpret the ROM as an electric circuit [3]. Note however that although the application of this BSP projector retains the block structure, each projected block becomes dense, and its inner structure is lost.

III. Simulation of the Reduced Order Model

Often, reduced representations are sought for modeling complex interconnect structures or electromagnetic coupling between blocks in a circuit. Full design analysis requires simulation of the design blocks together with the models of the relevant coupling or interconnect. In this section we will review some of the existing methodologies for the confinement of a projected ROM into a standard (SPICE-like) circuit simulator, in order to be simulated when coupled with other linear and non-linear circuitry.

A. Direct Use of the Reduced Order Model

The first and more straightforward approach is to directly plug the reduced model state space (4) representation into the circuit simulator. This is a natural approach, since these reduced models are already a compressed mathematical representation of the constitutive equations and conservations laws (i.e. a set of equations that drive the model behavior) relating the relevant variables. Such equations are in fact a representation exactly similar to the one that standard circuit simulators will use to generate stamps of the model, and couple them with the equations related to other circuit parts (both linear and non-linear). Some simulators allow the direct use of a state space representation (e.g. an NPORT instance in later versions of Cadence's SPECTRE [4]), whereby $\widehat{C}, \widehat{G}$ and $\widehat{B}$ are directly stamped on the circuit matrices or usage of an equivalent pole-zero representation (as in Synopsys's HSpice). However most of these approaches are tool-specific and not standartized, and there is no general agreement or how to input such data. Other simulators do not offer similar capabilities or do so in entirely incompatible fashion. Furthermore, many designers are not satisfied with such a solution and prefer to handle a netlist directly.

B. Circuit Interpretation

Another straightforward solution is to translate the reduced state space equations into an equivalent circuit representation which is then trivially ported to any analysis and simulation environment. This synthesis process is sometimes denoted as

Circuit Realization. As the ROM is directly interpreted as a (reduced) circuit. To understand how this interpretation is performed and the resulting circuitry, consider for example the i^{th} equation of the reduced model in (4) which would have the following structure

$$\hat{c}_{ii}\dot{\hat{x}}_i(t)+\hat{g}_{ii}\hat{x}_i(t) = \sum_{k=1}^{m}\hat{b}_{ik}u_k(t) - \sum_{j=1,j\neq i}^{q}\left(\hat{c}_{ij}\dot{\hat{x}}_j(t)+\hat{g}_{ij}\hat{x}_j(t)\right) \tag{6}$$

where $\hat{c}_{ij}$, $\hat{g}_{ij}$, and $\hat{b}_{ij}$ are the entries of the i-th row and j-th column of the dynamic ($\widehat{C}$), static ($\widehat{G}$) and I/O related ($\widehat{B}$) matrices respectively, and $\hat{x}_i$ is the i-th reduced state.

Realization via Controlled Sources

A straightforward possibility is to interpret (6) directly as a conservation equation and to build a circuit satisfying the exact same equation. This procedure can of course be repeated for all equations in (4). One could for instance equate $\hat{x}_i(t)$ as a node voltage of the desired circuit and interpret (6) as current balancing (KCL) at that node. In this case, terms on the left side of the equation can be readily implemented with a grounded capacitor ($\hat{c}_{ii}$) and resistor ($\hat{g}_{ii}$) and each of the terms on the right hand side of (6) can be realized through an appropriate (current or voltage) controlled current source. Even though this is a universal solution, in the sense that this solution can be confined into any SPICE-like circuit simulator, it is not a very efficient one, since for a q-order reduced model, whose matrices have q^2 entries (recall they are dense), it would require at least $2q^2$ controlled sources, plus q dummy capacitances and q dummy resistances. Further, controlled sources, while simple to understand, imply non-obvious relations between variables which are non-intuitive for designers and in this approach, the dynamics of all model states are directly dependent upon controlled sources. Such a solution is therefore also not very intuitive.

Hierarchical Preservation and Unstamping

Perhaps a more interesting set of approaches is based on the approach used to build the state space formulation from the circuit elements (the inverse operation with respect to circuit realization). These approaches try to revert the procedure, interpreting the elements of the reduced matrices as circuits elements, depending on their behavior and effect on the system equations. This procedure is also known as unstamping. For example, considering again Eqn. (6) and again assuming it represents current conservation at node i, if all the states are defined as voltages and the inputs as currents (a plausible and consistent interpretation), we can rewrite the equation so that

$$\begin{aligned}&-\textstyle\sum_{j=1,j\neq i}^{q}\left(\hat{c}_{ij}(\dot{\hat{v}}_i(t)-\dot{\hat{v}}_j(t))+\hat{g}_{ij}(\hat{v}_i(t)-\hat{v}_j(t))\right)+\\ &\dot{\hat{v}}_i(t)\left(\textstyle\sum_{j=1}^{q}\hat{c}_{ij}\right)+\hat{v}_i(t)\left(\textstyle\sum_{j=1}^{q}\hat{g}_{ij}\right)=\textstyle\sum_{k=1}^{m}\hat{b}_{ik}u_k(t)\end{aligned} \tag{7}$$

where $\hat{v}_j$ is the j-th node voltage. Examining (7), and specifically looking at the first term in the equation, each -$\hat{c}_{ij}$ can be interpreted as a capacitance between nodes i and j, and each -$\hat{g}_{ij}$ as a conductance between the same nodes. In order

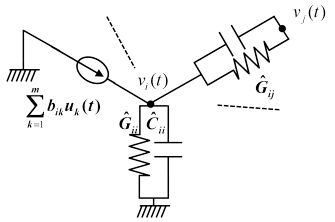

Fig. 1. Single node circuit interpretation.

to guarantee current conservation, we need to account for the second and third terms on the left side of the equation. To do this, we should add a grounded capacitance $\hat{c}_i = \sum_{j=1}^{q}\hat{c}_{ij}$, and a grounded conductance $\hat{g}_i = \sum_{j=1}^{q}\hat{g}_{ij}$ at node i. To guarantee current conservation, the equation would be complete by injection of external currents, provided by the $\hat{b}_{ik}u_k(t)$ terms on the right hand side. Figure 1 depicts the general idea in a simplified manner.

However, this approach has two major problems. The first one is related to the positivity of the elements and will be further illustrated below. The second one can be understood by recalling that the standard projection methodologies generates dense matrices, in which the inner structure is lost. This affects also the variables, since the new reduced set of states is a combination of the original states, both currents and voltages. Despite this, an interpretation in terms of electric elements, such as conductive (for $\widehat{G}$) and capacitive elements (for $\widehat{C}$), is possible as long as the matrices are symmetric (RC circuits lead necessarily to symmetric matrix formulations). This is true for the case of RC nets, but not for the general RLC case, in which $\widehat{G}$ is non-symmetric. In this situation, direct unstamping as described is not feasible (it is not possible to realize non-symmetric elements in $\hat{G}$ or $\hat{C}$ using only capacitors and conductances).

To overcome this issue, BSP approaches can be applied, so that the block hierarchy related to the variables in (1) is kept [3]. Therefore, the original block structure is still available after reduction, allowing a direct interpretation in terms of conductive, capacitive and inductive elements, from the reduced blocks related to the projection of $\mathcal{G}$, $\mathcal{C}$ and $\mathcal{L}$, respectively, in (1). It is important to notice that the same interpretation can be obtained from the standard projection of a second order system (3).

Therefore, for a block size q, direct unstamping will generate $(q^2+q)/2$ resistors, $(q^2+q)/2$ capacitors, and $(q^2+q)/2$ inductors. In addition, since the I/O related reduced matrix block $\mathcal{B}$ is full, the distribution of the m inputs into the unstamped netlist requires mq controlled sources, and the combination of the responses into the m outputs require another mq controlled sources. However, we should note that such source are used only in relation to input and output, namely to weigh in the inputs at each node and to sum up voltages at the output. They are not directly related to the circuit dynamics (time constants, eigenvalues) which can be directly obtained from the capacitive and conductive elements of the circuit. As such the existence of such sources is considered a minor inconvenience.

To avoid the use of controlled sources, some methods advocate for the preservation of the I/O nodes [5], [6]. These methods rely on the fact that the ports usually are only a small fraction of the circuit nodes. This block of nodes can be left unreduced by a BSP approach, in which a Identity block is used instead of a projector for such block. The work in [5] further proposes a diagonalization of the inductive block based on an Schur decomposition. This diagonalization allows to avoid inductive loops in the unstamped circuit, and, if no inductors are directly connected to the ports, do not affect the preservation of the I/O blocks. This approach allows to generate an equivalent circuit with $(q^2+q)/2$ resistors and $(q^2+q)/2$ capacitors, plus q ground inductors.

The main problem with these approaches is that the orthogonal projection, despite guaranteeing the passivity preservation for MNA based formulations, does not guarantee that the unstamped individual R, L and C elements are positive, which can raise problems in certain simulators (and is completely non-intuitive). Experience indicates that in practice, quite often, the unstamped elements are indeed not all positive. To illustrate this issue we present a small randomly generated RC example, composed of 5 capacitors and resistors. The matrices involved in the MNA equations for this circuit are

$$G=\begin{bmatrix} 2 & -1 & 0 \\ -1 & 3 & -0.1 \\ 0 & -0.1 & 1.8 \end{bmatrix} \quad C=\begin{bmatrix} 2.2 & -1.8 & 0 \\ -1.8 & 2.5 & -0.6 \\ 0 & -0.6 & 1 \end{bmatrix} pF \tag{8}$$

with a single port connected to node 1. If we generate a projector V with an orthonormal basis of the first two moments of the transfer function of such system at zero ($M_0 = G^{-1}B$, and $M_1 = G^{-1}CM_0$), the projected matrices are

$$G=\begin{bmatrix} 1.498 & -0.477 \\ -0.477 & 3.233 \end{bmatrix} \quad C=\begin{bmatrix} 1.142 & -1.339 \\ -1.339 & 2.877 \end{bmatrix} pF \tag{9}$$

both symmetric and positive semidefinite (PSD), and thus the system is passive. However, direct unstamping of (9) as described previously leads to a two node circuit with grounded resistors and capacitors at each node $r_1 = 0.979$, $c_1 = -0.198$pf and $r_2 = 0.362$, $c_2 = 1.538$pf, and another resistor and capacitor connecting both nodes $r_{12} = 2.096$, $c_{12} = 1.339$pf. Even in this small and simple example the projection leads to a negative capacitor (it would have been possible to enforce all grounded capacitors to be positive, but then the floating capacitor between nodes 1 and 2 would be negative). For larger and more complex examples the issue is quickly aggravated.

C. Transfer Function Realization

Yet a different approach to circuit realization is based on a pole and zero (or pole and residue) rational representation of the reduced model

$$\widehat{H}(s) = \sum_{i=1}^{q} \frac{r_i}{s-p_i} \tag{10}$$

where $r_i \in \mathbb{C}$ are the residues and $p_i \in \mathbb{C}$ are the poles. The work in [7] presents a review of methodologies which used this pole-zero formulation to synthetize a circuit using controlled sources. Following a different direction, the work proposed in [8], [6] interprets each SISO transfer function as a set of parallel admittances or serial impedances, depending on the nature of the input and the output, where each admittance/impedance corresponds to a term in (10). Real poles and residues can be realized as a simple RC element, whereas complex conjugate pairs can be realized into a more complex RLC element. Since this approach is SISO oriented, the complete MIMO system must be assembled as a combination of all input-output pairs realization. However, the main problem associated with this approach is again that the synthetized R, L and C elements can be negative, and thus raises problems when used with certain circuit simulators.

An approach leading to a circuit where all elements are guaranteed positive (i.e. physical) is more interesting as it is more intuitive to reason with.

IV. Positive RLCM Generation

In this section we introduce the proposed approach for the generation of equivalent circuits with positive elements, and thus able to be confined in any SPICE-like circuit simulator.

The basic idea of this method is to ensure that all elements in equivalent RLC netlist, are guaranteed to be positive, whereas the I/O relation is kept by a set of current and voltage controlled sources. As discussed, since such sources do not directly determine local dynamics, their presence is considered a minor inconvenience.

A. Coordinate Transformation and Diagonalization

The first part of the framework relies on a coordinate transformation to diagonalize some reduced matrix blocks. We start from a (reduced) second order system representation,

$$\left(s\widehat{\mathcal{C}} + \widehat{\mathcal{G}} + \tfrac{1}{s}\widehat{\mathcal{K}}\right)\widehat{x}(s) = \widehat{\mathcal{B}}u(s), \quad y(s) = \widehat{\mathcal{B}}^T x(s), \tag{11}$$

where $\widehat{\mathcal{C}}$, $\widehat{\mathcal{G}}$, $\widehat{\mathcal{K}} \in \mathbb{R}^{q\times q}$ and $\widehat{\mathcal{B}} \in \mathbb{R}^{q\times m}$ are dense matrices, generated by a congruence projection, and thus $\widehat{\mathcal{C}}$, $\widehat{\mathcal{G}}$, $\widehat{\mathcal{K}}$ are symmetric semidefinite positive (SDP) matrices. An equivalent block reduced first order formulation can also be used with exactly the same result.

We perform an eigenvalue decomposition on the $\widehat{\mathcal{G}}$ matrix, $X_g\widehat{\mathcal{G}} = X_g\Sigma_g$. Since $\widehat{\mathcal{G}}$ is symmetric and SDP, the eigenvalues are real positive, and $X_g^{-1} = X_g^T$, so $\widehat{\mathcal{G}} = X_g\Sigma_g X_g^T$ (notice that applying a Singular Value Decomposition (**SVD**) on $\widehat{\mathcal{G}}$ would generate a similar result).

We can then rewrite the system as

$$\left(sT_g^T\widehat{\mathcal{C}}T_g + I + \tfrac{1}{s}T_g^T\widehat{\mathcal{K}}T_g\right)x = T_g^T\widehat{\mathcal{B}}u, \quad y = \widehat{\mathcal{B}}^T T_g x \tag{12}$$

with $T_g = X_g\Sigma_g^{-1/2}$, and I the identity. If now we perform another eigendecomposition on the matrix $T_g^T\widehat{\mathcal{C}}T_g$ (which is also symmetric positive definite), we have $T_g^T\widehat{\mathcal{C}}T_g = X_c\Sigma_c X_c^T$. Applying a new congruence transformation with the matrix $T_c = X_c$, we can again rewrite the system as

$$\left(s\Sigma_c + I + \tfrac{1}{s}T_c^T T_g^T\widehat{\mathcal{K}}T_g T_c\right)x = T_c^T T_g^T\widehat{\mathcal{B}}u, \quad y = \widehat{\mathcal{B}}^T T_g T_c x \tag{13}$$

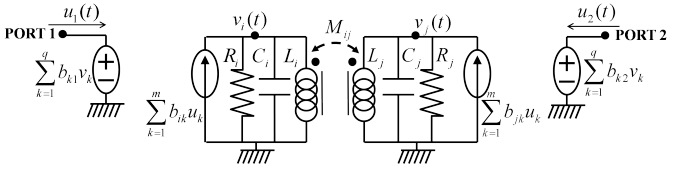

Fig. 2. Example of schematic of the proposed synthesis, with 2 ports and current injection (only two nodes, i and j are represented). Each node will be composed of a R, L and C in parallel, fed by a set of m parallel current controlled current sources (here presented as a sum), each injecting the current of the m-th port weighted by the corresponding IO matrix element. The resulting voltage in each of the q nodes is sum weighted by the corresponding IO matrix entry, via a set of serial voltage controlled voltage sources, to generate the corresponding voltage at each port.

where Σ_c is a diagonal matrix with positive real values, and I is the identity matrix. If we rename $\bar{G} = I$, $\bar{C} = \Sigma_c$, $\bar{K} = T_c^T T_g^T \widehat{\mathcal{K}} T_g T_c$, and $\bar{B} = U_c^T T_g^T \widehat{\mathcal{B}}$, we obtain the system

$$\left(s\bar{C} + \bar{G} + \tfrac{1}{s}\bar{K}\right) x = \bar{B}u, \quad y = \bar{B}^T x, \tag{14}$$

which is equivalent to projecting the original reduced system with $X_g \Sigma_g^{-1/2} X_c$.

B. Interpretation and Realization

The congruence transformations do not affect the positive definiteness of the system matrices, which remain SDP. The conductance and capacitance matrices, $\bar{G}$ and $\bar{C}$, are diagonal with positive diagonal values, and thus can be directly unstamped as a set of (positive) resistors and capacitors connected to ground.

The matrix $\bar{K}$ is also SDP, and thus can be inverted to generate the inductive elements. This inverted matrix L is also SDP, which means that its diagonal entries l_{ii} are positive, and in addition the off-diagonals satisfy $|l_{ij}| \leq \sqrt{l_{ii} l_{jj}}$. Therefore, the diagonal elements can be interpreted as a set of positive inductances connected from each node to ground, whereas the off-diagonals can be interpreted as mutual inductors, coupling each pair of inductances with absolute values ≤ 1.

The I/O matrix $\bar{B}$ is a dense matrix with different values, and thus the I/O connection should be made via a set of mq current controlled current sources to distribute the current to every node, and mq voltage controlled voltage sources to retrieve the voltage on the nodes.

Therefore, the complete circuit can be represented by q subcircuits, each of them consisting of a current controlled current source that feeds one resistor, one capacitor and one inductor connected in parallel to ground. In addition, each inductance is coupled to the remaining $q-1$ inductances via a mutual inductance (with a total of $(q^2-q)/2$). All RLC values are positive, and the mutual inductance couplings have an absolute value less than 1. The circuit also needs mq voltage sources controlled by the voltage on the nodes, and which generate the output voltage. A depiction of the proposed synthesis is given in Figure 2.

C. Circuit Characteristics and Computational Issues

Since the procedure outlined above is based upon operations using algebraic full rank transformations, the equivalent system generated has the following characteristics:

- All system matrices remain symmetric SDP, and thus the system is passive.
- All the synthetized elements can be used in any SPICE-like circuit simulator: only positive resistors, positive capacitors, positive inductors, and mutual inductors with absolute values ≤ 1 are generated, plus controlled sources.
- The stamp of the equivalent circuit generates sparse matrices, and thus can be efficiently simulated (small penalty when compared with [5] but no negative elements).
- The synthesis is very economic, requiring only q resistors, capacitors and inductors, plus $(q^2-q)/2$ mutual inductances and $2mq$ controlled sources.
- The use of mutual inductances and controlled sources make the equivalent circuit free of inductance loops.
- I/O accuracy is maintained since only full-rank algebraic transformations have been applied.

Furthermore the structure of the resulting circuit makes it very intuitive for reasoning with the various elements.

V. Simulation Results

This section will validate and illustrate the statements presented along the manuscript. In order to compare the proposed approach, we use a set of different benchmarks. **RC** is a NA model of a 5 line bus, in which each line is modeled by a distributed RC model, with p.u.l. values for the R and C elements of each of the 1000 segments used, as well as for the coupling capacitances that model the line cross-talk. The complete system can be modeled as a 5010 state space, and each line termination is taken as a port, so the complete system has 10 terminals. **RLC** is a MNA model of a similar 5 line bus, but in this case each line segment is modeled by a distributed RLC model, with p.u.l. values for the R, L and C elements of each of the 400 segments used. The coupling between the lines is also modeled by cross capacitances and mutual inductances. The complete system can be modeled as a 6010 state space, and each line termination is taken as a port, so the complete system has 10 terminals. These two examples are similar to those used presented [7]. **IND1** and **IND2** are two realistic examples provided by **HELIC Inc**. Each of them is an extracted netlist of two different octagonal integrated inductors, one with 5 and the other with 7 turns, and different geometric characteristics. The netlists, composed of resistors, capacitors, inductors and mutual inductances, were generated using HELIC's **VELOCE RF** tool [9]. Each model has two ports modeling the inductor terminals. Each model was reduced using the PMTBR approach [2], which relies in sampling the frequency domain for the generation of a suitable orthogonal basis. The approach was combined with a BSP projection, to generate the ROM that was used as starting point for the synthesis. The size of ROM was fixed so that all the reduced models have near perfect accuracy.

TABLE I
RESULTS OF THE SYNTHESIS AND THE SIMULATION OF THE EQUIVALENT NETLISTS

	Model	Ports	R (neg.)	C (neg.)	L (neg.)	M	CCCS	CCVS	Time (s)	Mem. (MB)
RC	Original	10	10025 (0)	15010 (0)	0 (0)	0	0	0	6.47	32.1
	Unstamping	10	195 (79)	76 (32)	0 (0)	0	0	0	0.06	4.06
	Foster	10	1020 (438)	1100(474)	0 (0)	0	100	100	0.38	7.03
	Proposed	10	11 (0)	11 (0)	0 (0)	0	110	110	0.10	4.21
RLC	Original	10	4025 (0)	6010 (0)	2000 (0)	4000	0	0	7.72	23.9
	Unstamping	10	1130 (562)	751 (365)	38 (0)	0	0	0	0.680	5.87
	Foster	10	7600 (4080)	5697 (2457)	1903 (843)	0	100	100	28.50	26.7
	Proposed	10	38 (0)	38 (0)	38 (0)	703	380	380	1.02	6.04
IND1	Original	2	457 (0)	256 (0)	380 (0)	2850	0	0	4.88	8.31
	Unstamping	2	119 (54)	136 (61)	29 (9)	0	0	0	0.06	4.07
	Foster	2	115 (48)	92 (38)	20 (6)	0	4	4	0.08	4.07
	Proposed	2	14 (0)	14 (0)	14 (0)	91	28	28	0.09	3.94
IND2	Original	2	650 (0)	374 (0)	540 (0)	5778	0	0	12.160	11.8
	Unstamping	2	378 (191)	406 (201)	53 (23)	0	0	0	0.180	4.61
	Foster	2	208 (102)	160 (74)	48 (18)	0	4	4	0.120	4.34
	Proposed	2	26 (0)	26 (0)	26 (0)	325	52	52	0.210	4.34

The approaches used for the synthesis were a IO preservation and unstamping process as presented in [5], labeled as **Unstamping**, a Foster's equivalent synthesis based on pole-residue analysis and realization as presented in [6], labeled as **Foster**, and the proposed positive RLCM methodology presented in Section IV, denoted as **Proposed**. Note that in order to apply the IO preservation for the unstamping process, the same projector was further expanded into a port preserving one, which resulted in an increment of the number of nodes. The Foster synthesis is a single-input single-output transfer function realization. Since each SISO transfer function is an impedance, the combination of the m^2 SISO circuits into the overall MIMO circuit requires an additional set of $2m^2$ controlled sources.

Table I shows the characteristics of the original models, as well as the characteristics of the synthesized netlists. It presents the number of ports and the number of elements of each netlist, namely resistors (R), capacitors (C), inductors (L), mutual inductors (M), current controlled current sources (CCCS), and voltage controlled voltage sources (VCVS). In the case of R, C and L, the numbers between parenthesis indicate the number of negative resistors, capacitors and inductors, respectively. We have also included the elapsed time and memory required for a simulation in SPECTRE RF [4], for a transfer function analysis (XF) of 1000 points.

It can be seen that both unstamping and Foster realization retrieve negative elements, and thus such realizations cannot be used in most of the simulation environments (SPECTRE allows the use of negative elements, generating a warning for each negative element found). On the other hand, the proposed approach is free of such negative elements for all cases. For that we must pay a small penalty in the number of controlled sources used, which is translated into a higher number of nodes. However, it can be seen that the simulation time and memory increase is not very relevant, in particular if compared to the fact that the competing models are unusable in some simulation environments.

VI. CONCLUSIONS

This paper proposes a methodology for the synthesis of reduced order models of general multiport RLCM nets amenable to be included in standard simulation environments. Unlike other previously published approaches, the methodology generates very compact models containing guaranteed positive R, L, and C elements, plus mutual inductances and a set of controlled sources to assemble the overall IO. Such a representation can be directly included in any SPICE-like circuit simulator.

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