

A VERY LOW-POWER CMOS PARALLEL A/D CONVERTER FOR EMBEDDED APPLICATIONS

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ABSTRACT

We present a new pseudo-differential comparator block that behaves like a comparator array, but has reduced area, power consumption, and input capacitance. By combining two of the new comparator blocks with input sample and hold circuits, in an interleaving architecture, and by using a Wallace-tree encoder, it is possible to obtain an ADC with limited resolution (up to 6 bits), but with very low power consumption, and also with low area and low supply voltage. As an example, we have designed a 4-bit ADC to be embedded as a coarse converter in a 13 bit pipeline ADC. It is implemented in a 0.35 μm CMOS technology, has 0.034 mm² and has power consumption of 210 μW , with an estimated input capacitance of 11 fF.

1. INTRODUCTION

Comparators are used in parallel type ADCs [1], where the large number of comparators makes them the main contributors to the overall area and power consumption. Usually a differential pair is used as the input stage of each comparator, in which a single ended input is compared with a reference voltage. To compare the ADC input voltage with several reference voltages simultaneously an array of comparators is required, which increases the area and input capacitance.

We present a new pseudo-differential comparator block that performs the same function as an array of n comparators with a common input and n reference voltages, but has lower area, power consumption, and input capacitance.

By applying two complementary balanced input voltages to a pair of these new blocks, both having the same n reference voltages, it is possible to realize the same function as an array of $2n$ comparators with $2n$ reference voltages, and with an input range which is twice that of the individual blocks. Finally, by using two sample and hold circuits at the input of the two blocks, it is possible to have interleaved operation, at the cost of only one additional input transistor in each block. The

sample and hold circuits use low power amplifiers, since their load is the new comparator block, which has a very low capacitance input. Thus, a very low-power ADC front-end is obtained.

Further area and power savings can be obtained by using a Wallace-tree encoder [2], which performs error correction in an efficient way. As a consequence, larger offset voltages can be allowed in the comparator blocks, which can be designed with smaller transistors and lower currents. The result is a very low power ADC.

The resolution of the new comparator block is limited due to the effect of transistor mismatches. It is reasonable to expect that this limitation is similar to that which applies to a set of individual pseudo-differential comparators. The resolution is reduced for low supply voltage (it is expected that up to 6 bits may be obtained with 1.5 V supply).

As an example of application of the techniques proposed in this paper, we present here a 4-bit ADC which is to be used in the front-end of a two channel, 1.5 V, 13 bit, 130 MS/s self-calibrated pipeline ADC using only 1 pJ of energy per conversion [3]. This application imposes severe restrictions on power consumption and on input capacitance with a high sampling frequency.

Although the new comparator block was developed for this specific application, it can be used in many other applications where low resolution (4-6 bit) ADCs are required, in the MHz range, either with or without a sample-and-hold circuit, and where low-power consumption is the most important requirement. Another example is low-IF or baseband analog-to-digital conversion for wireless receivers [4].

In section 2 we present the new pseudo-differential comparator block. In section 3 we show how to use two blocks with a balanced input signal. In section 4 it is shown how the new comparator block can be adapted for interleaved architecture. In section 5 we describe the 4-bit ADC, using pseudo-differential comparator blocks as the analog part, and a Wallace-tree encoder as the digital part. In section 6 we present simulation results, and in section 7 we draw some conclusions.

2. PSEUDO-DIFFERENTIAL COMPARATOR BLOCK

The pseudo-differential comparator block is represented in Fig.1. It is inspired by the pseudo-differential pair [5], which differs from the usual emitter-coupled pair by suppressing the tail current source. It is assumed that the PMOS and NMOS transistors are matched i.e., $V_{ip} = V_{in}$ and $\mu_n C_{ox} (W/L)_n = \mu_p C_{ox} (W/L)_p$. If the transistors are in the saturation region, it is easy to show that the output voltage, V_{OUTi} is $V_{DD}/2$ for $v_{IN} = V_{Ri}$.

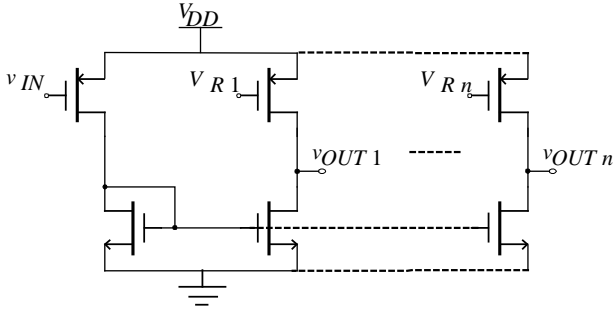


Fig. 1: Pseudo-differential comparator block.

The main reason for using the conventional differential pair (with a tail current source) is that it ensures common mode voltage rejection and that the transconductance of the differential pair is independent of the reference voltage value, within certain bounds. For the proposed circuit the common mode voltage rejection is not an issue, since the reference voltage is known from the beginning. The transconductance will be different for each output. The transition delays are also different, which limits the frequency to a few MHz (this depends on supply voltage, input range and transistor dimensions), since the input signal is not allowed to vary significantly while the different transitions are taking place. However, if a sample-and-hold is used, the different delays are not relevant, and the sampling frequency will only be limited by the delay of the slowest output.

The pseudo-differential comparator block in Fig. 1 performs the same function as an array of n individual comparators with a common input and with n different reference voltages.

3. TWO BLOCKS WITH BALANCED INPUTS

We can connect two of the comparator blocks in Fig. 1 as shown in Fig. 2. The two blocks have the same reference voltages and their inputs are balanced, i.e., they are of the form $V_C + v_d$ and $V_C - v_d$, where V_C is a constant common-mode voltage.

The transfer curves in Fig. 2 are a simplified representation (step transition) of the real curves (gradual transition). One of the blocks provides outputs with transitions situated in one half of the input range, and the other block provides the transitions in the other half of the input range.

The transfer curves in Fig. 2 show that the set of two blocks with $n+1$ and n reference voltages is equivalent to, (i.e., perform the same function as) an array of $2n+1$ individual comparators with $2n+1$ reference voltages.

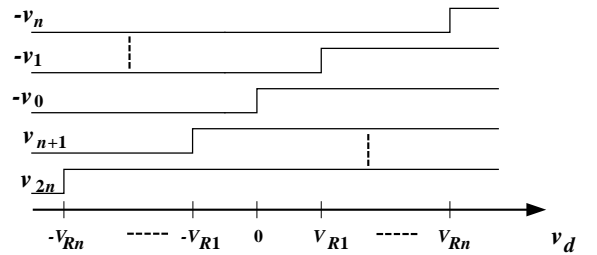
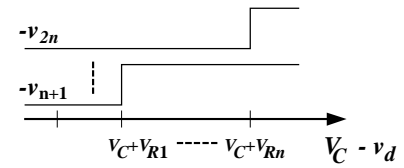
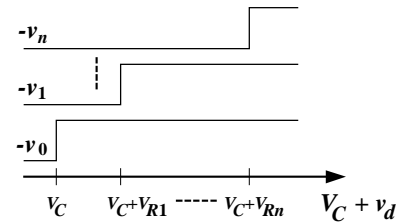
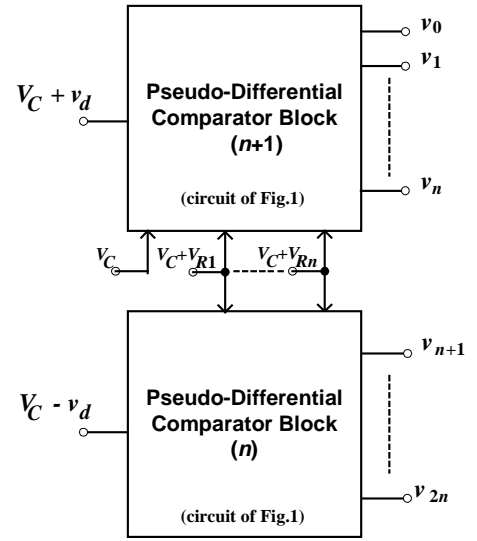


Fig. 2: Two comparator blocks with balanced inputs.

4. INTERLEAVING ARCHITECTURE

An ADC with interleaving architecture [1] is represented in Fig. 3. The sample and hold circuits provide balanced outputs. Each circuit is active (provides sampled and held balanced signals at the outputs) during about half of the sampling period, while the other circuit is inactive, (with both outputs at the supply voltage level V_{DD}).

The comparator blocks in Fig. 3 have dual input by adding one transistor at the input of the circuit in Fig. 1, as shown in Fig. 4. One of the input transistors is off, when the corresponding sample and hold circuit is inactive (with V_{DD} at their outputs). By using this arrangement, we can have interleaving and the resulting increase of the speed of operation, without having to double the number of comparator blocks.

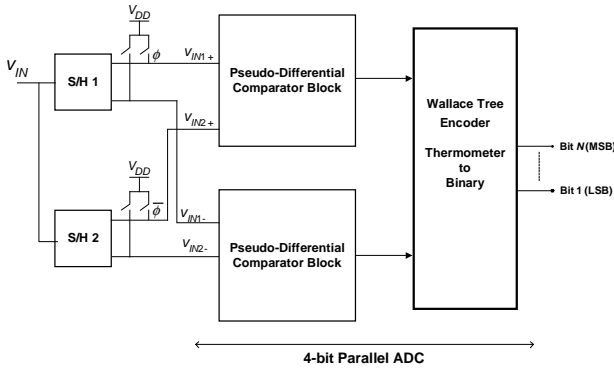


Fig. 3: Block diagram of an interleaved ADC

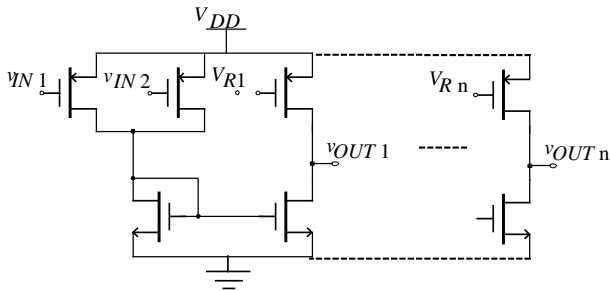


Fig. 4: Pseudo-differential comparator block with dual input for interleaved architecture.

5. A 4-bit ADC

5.1 ADC Specifications

To demonstrate the use of the design techniques described above we have designed a 4-bit parallel ADC, with the architecture represented in Fig. 3, to be used, as one block, in a two-channel pipeline ADC. Although the techniques presented in the previous sections can be used

in other applications, the original motivation was to meet the target specifications in Table 1.

Table 1: 4-bit ADC Specifications

Sampling Frequency	65 Ms/s (two channels)
Resolution	4 bit
Supply Voltage	1.5 V
Settling time	7.7 ns
Power consumption	< 13 mW
Input range	0.25 V-1.25 V (differential)
Technology	0.35 μ m CMOS

Due to the low supply voltage, the differential input signal is almost rail-to-rail. This is a low resolution ADC (4 bits). A low input capacitance is needed to relax the S/H specifications.

5.2 ADC Design

The ADC has the architecture represented in Fig. 3 and is implemented with a 0.35 μ m CMOS technology. The dimensioning is straightforward. The output voltage should be $V_{DD}/2$ which defines the ratio $(W/L)_{PMOS} / (W/L)_{NMOS}$; we can increase W/L to reduce mismatch, either maintaining the W/L or increasing W of both transistors. Power will increase, but the settling time will be reduced. The dimensions of the transistors of the pseudo-differential comparator are: $(W/L)_{PMOS} = (3.6 / 1.0)$; $(W/L)_{NMOS} = (1.2 / 1.0)$. These values are 3 times the minimum dimensions in order to ensure a precision higher than $1/2$ LSB, in spite of mismatches.

The outputs of one of the comparator blocks must be inverted (see lower set of curves in Fig. 2); for this purpose we use CMOS inverters with matched transistors (two inverters in cascade are used to shape the outputs of the other block).

The encoder is a Wallace-tree encoder, which is an alternative to the commonly used ROM encoders: instead of determining the 0 to 1 transitions, the number of ones is counted, providing error correction, and reducing the errors due to glitches, or due to deterministic errors, like offset voltages [2]. The Wallace-tree encoder, represented in Fig. 5, requires only eleven full-adders. Due to the sample-and-hold circuits at the input, we only use 4 latches at the outputs instead of a much larger number of latches at the encoder inputs.

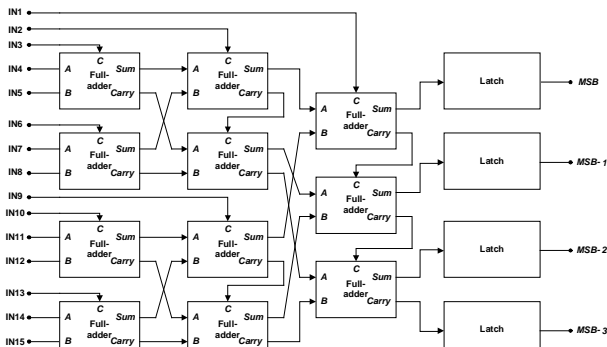


Fig. 5: Wallace-tree encoder for 4 bit ADC.

6. SIMULATION RESULTS

Without mismatches the INL is lower than 0.15 LSB and the DNL is lower than 0.2 LSB. With mismatches a Monte Carlo analysis shows that the values remain under $\pm 1/2$ LSB, which is the maximum value allowed by the specifications. In Fig. 6 we show the ADC output waveforms obtained by a Monte Carlo analysis. The layout, represented in Fig. 7, has with $150 \mu\text{m} \times 220 \mu\text{m}$.

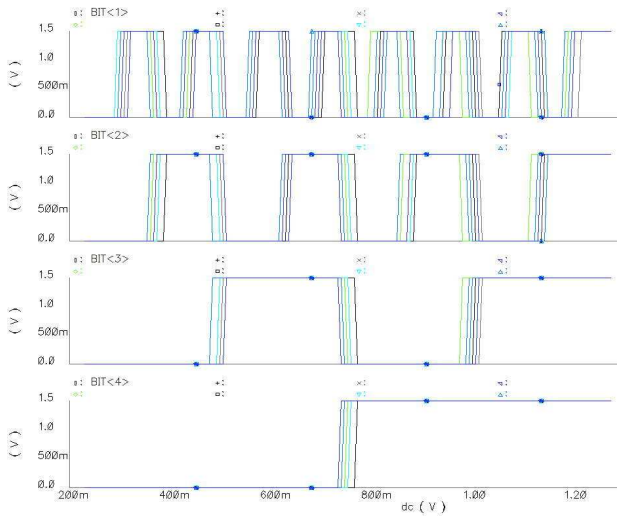


Fig. 6: Monte Carlo analysis for 4 bit ADC

The designed ADC has the following characteristics:

Sampling Frequency	135 MHz
Resolution	4 bit
Input signal range	0.5V x 2
Input capacitance	≈ 11 fF
Supply Voltage	1.5 V
Power consumption	210 μW
	(average for full scale input)
INL and DNL (Monte Carlo)	< 0.5 LSB
Area	0.034 mm^2

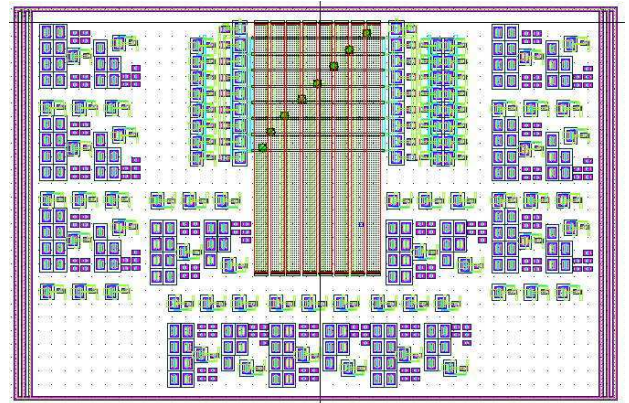


Fig. 7. 4-bit ADC layout (routing not shown).

7. CONCLUSIONS

We describe new techniques to realize low resolution ADCs with very low power and area, and also with low supply voltage. These techniques are based on a new circuit, the pseudo-differential comparator block, which has low input capacitance. We also present an architecture that makes full use of the new block possibilities. As an example we present a 4-bit ADC to be embedded in a two-channel pipeline ADC. The 4-bit converter has an area of 0.034mm^2 and consumes $210 \mu\text{W}$ with a supply voltage of 1.5 V. The estimated input capacitance is 11 fF. Simulations that include Monte Carlo analysis confirm the expected circuit performance.

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