Test Results of an ITER Relevant FPGA when Irradiated with Neutrons

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Abstract—The data acquisition and control instrumentation in port cell cubicles of tokamak ITER will be irradiated with neutrons, during the fusion reactor operation. A Virtex-6 FPGA from Xilinx (XC6VLX365T-1FFG1156C) is used on the ATCA-IO-PROCESSOR board, included in the ITER Catalog of I&C products - Fast Controllers. The Virtex-6 is a re-programmable logic device where the configuration is stored in Static RAM (SRAM), functional data stored in dedicated Block RAM (BRAM) and functional state logic in Flip-Flops. Single Event Upsets (SEU) due to the ionizing radiation of neutrons causes soft errors, unintended changes (bit-flips) to the values stored in state elements of the FPGA. The SEU monitoring and soft errors repairing, when possible, were explored in this work. An FPGA built-in Soft Error Mitigation (SEM) controller detects and corrects soft errors in the FPGA configuration memory. SEU sensors with Error Correction Code (ECC) detect and repair the BRAM memories. Proper management of SEU can increase reliability and availability of control instrumentation hardware for nuclear applications. The results of the tests performed using the SEM controller and the BRAM SEU sensors are presented for a Virtex-6 FPGA (XC6VLX240T-1FFG1156C) when irradiated with neutrons from the Portuguese Research Reactor (RPI), a 1 MW nuclear fission reactor operated by IST in the neighborhood of Lisbon. Results show that the proposed SEU mitigation technique is able to repair the majority of the detected SEU errors in the configuration and BRAM memories.

I. INTRODUCTION

The ITER tokamak will be a nuclear fusion reactor confining a considerable amount of energy during the one hour operation period. As a consequence a plasma disruption (confined energy suddenly released) can generate enough forces to cause damage to the vessel and other structures. To avoid plasma disruptions the ITER control hardware must withstand the magnetic field and ionizing radiation generated during the steady state discharge. The ITER port cell cubicles, for the data acquisition and control instrumentation, will be irradiated with neutrons during the tokamak operation. The expected neutrons energies are mainly of 14 MeV and 100 keV with fluxes around $10^3 \text{n/cm}^2/\text{s}$ and $10^5 \text{n/cm}^2/\text{s}$ respectively [1]. The ITER Catalog of I&C products - Fast Controllers [2] contains instrumentation based on Field Programmable Gate Arrays (FPGA) and the effects of the ionizing radiation due to neutrons must be evaluated.

A Virtex-6 FPGA (XC6VLX365T-1FFG1156C) from Xilinx is used on the ATCA-IO-PROCESSOR board [3] of the ITER fast controllers catalog. To perform the tests to the FPGA a Xilinx development kit (ML605) [4] was used since has a lower cost relatively to the ATCA-IO-PROCESSOR board. The development kit contains an FPGA of the same family (XC6VLX240T-1FFG1156C) allowing cheaper preliminary tests in case of board damage and activation due to the neutrons radiation.

The Virtex-6 FPGA is a re-programmable logic device where the configuration is stored in Static RAM (SRAM), functional data stored in dedicated Block RAM (BRAM) and functional state logic in Flip-Flops. Neutron radiation can induce Single Event Upsets (SEU), also known as soft errors or bit-flips, in the state elements of the FPGA. In this work the SEU detection and respective errors correction in the FPGA state elements (except functional Flip-Flops) were tested, using a Soft Error Mitigation (SEM) controller and BRAM SEU sensors with hard Error Correction Code (ECC).

II. EXPERIMENTAL SETUP

The tests have been performed on the Portuguese Research Reactor (RPI), a 1 MW nuclear fission reactor operated by IST in the neighborhood of Lisbon. The reactor irradiation facility used was the fast neutron beam tube E4 and respective chamber [5]. Fig. 1 shows the layout of the RPI fast neutrons irradiation facility E4.

![Fig. 1. RPI fast neutrons irradiation facility E4, showing: (a) irradiation chamber at the exit of neutron beam tube; (b) prolongation inside the tube; (c) neutron and gamma filter; (d) periphery of the fission reactor core inside the water cooling/shielding pool.](image)
As the tests needed to be scheduled accordingly with the agenda availability, of RPI fast neutrons irradiation facility, the experimental setup was planned to be monitored and operated remotely using the internet. In this way numerous journeys between IPFN and RPI site have been avoided.

The AC power supplies of the experimental equipment were independently ON/OFF controlled allowing recovering from possible failures, e.g. PCs or FPGA board crashes.

The experimental setup, Fig. 2, comprises an irradiation chamber (Fig. 3), a Xilinx ML605 board with the FPGA (XC6VLX240T-1FFG1156C) to test, communications and power cabling (electrical and optical), an ON/OFF controller (APC AP7920) for the AC power supplies of the equipment, an Ethernet switch and two PCs.

One of the PCs (Windows OS) was used for the FPGA programming and also to run the software needed for the monitoring and execution of BRAM SEU and SEM tests. The other PC (Linux OS) was running the ITER data acquisition software of the ATCA-IO-PROCESSOR board [6].

The standard EIA-232 communications between the PC and the UART of the FPGA have been used for the BRAM SEU and SEM tests.

FPGA programming and configuration read-backs were done through the Xilinx JTAG tool.

Optical PCI express communications between the ITER data acquisition PC and the FPGA were used to emulate the Advanced Telecommunications Computing Architecture (ATCA) based infrastructure, which normally hosts the ATCA-IO-PROCESSOR board [7]-[8].

A. FPGA Firmware

The firmware implemented for the tests includes three main blocks, a SEM controller, 220 sensors for BRAM SEU detection and the ITER data acquisition logic. Fig. 4 shows the FPGA firmware diagram and respective board interfaces used.

The SEM controller is a Xilinx IP core [9] that was configured to implement the initialization, SEU error detection and SEU error correction. The core utilizes the device primitives ICAP and Frame_ECC to clock and observe the read-back CRC circuit as part of the SEU detection function. For the configuration memory SEU correction the IP core performs the necessary operations to locate and repair the error (scrubbing).

The SEM controller initializes by bringing the integrated soft error detection capability of the FPGA into a known state. After this initialization, the SEM controller observes the integrated soft error detection status. When an ECC or CRC error is detected, the SEM controller try to identify the configuration memory location involved. If the location can be identified, the SEM controller corrects the soft error by repairing it. The repair method use active partial reconfiguration to perform a localized correction of the configuration memory using a read-modify-write scheme. The repair consists of correcting one bit per configuration memory frame and per scrubbing cycle. If two or three error bits are detected the SEM controller stops. Above three soft errors bits the SEM controller can be not able to detect them.
The SEM controller does not operate on soft errors in BRAMs, distributed memory, or flip-flops. Soft error mitigation in these memory resources need to be addressed by the user logic through preventive measures such as redundancy or error detection and correction codes, which is out of the scope of this work.

SEU sensors for events detection in the functional memory were implemented (220 sensors). Each sensor consists on an available ECC hard core, free BRAM and a counter [10]. The counter counts the number of detected errors (the SEU events in the BRAM blocks). As the SEM controller the SEU BRAM based sensors do the repair of one soft error bit, if two or three errors happen the SEU sensor continues to work but no correction is made. As the SEM controller above three error bits the BRAM SEU sensor cannot be able of doing the soft errors detection.

The SEM controller needs less than 15 ms to do the error detection/repair of one frame in the configuration memory and the BRAM SEU sensor needs less than 2 μs for the equivalent.

The ITER data acquisition firmware was implemented without SEU detection and respective soft error correction. The aim was to occupy the FPGA resources and to operate in similar conditions as the ITER FPGA. The total used FPGA logic resources have been: 93215 Registers (30%); 80725 LUT (53%); 30087 Slices (79%); 363 BRAM (87%); 211 DSP48E1 (27%); 3 MMCM (25%); 13 Bufg (40%); 1 GTXE1 (5%); 1 ICAP (50%); 1 PCIe_2_0 (50%). FPGA operation temperature was ~60 °C. To understand the meaning of the acronyms above for the FPGA resources please consult [11].

B. Test Software

The SEU test software was a terminal running on a PC, with Windows OS, and connected by USB to the UART of the FPGA. In the terminal window the configuration memory SEU counter and the BRAM sensors SEU counter are updated in real time.

The Xilinx JTAG with respective Impact software was used for the FPGA programming and configuration read-back. FPGA temperature, currents and voltages monitoring was also done using JTAG and Impact software.

The ITER data acquisition software was an EPICS application running on a PC, with Linux OS, and connected by PCI Express to the FPGA endpoint. The software displays in real time blocks of the acquired data. The acquired data was internally generated by an FPGA counter to simulate a digitized saw-tooth waveform.

III. TESTS RESULTS

The neutron spectrum at the irradiation facility E4 is a fission spectrum, with maximum intensity around 2 MeV and a maximum practical energy around 17 MeV [12] that includes the energies and fluxes (reactor operating power dependent) expected in the ITER port cell cubicles. Since the neutron spectrum is wide, other neutrons energies are present and have the bigger contribution to the FPGA SEU results attained in the tests performed for this work. For 1 MW reactor operation the total flux at the irradiation chamber beam tube exit is \(2.74 \times 10^8\) n/cm\(^2\)/s, the total neutron flux decreases linearly with the reactor operating power.

Two different irradiation test approaches have been done, one was the FPGA not running (clocks stopped) with configuration and functional memory read-back. The other was SEU detection with error correction in real time when the FPGA is running. The results for the two approaches have been then compared for results validation.

The FPGA irradiation results are shown in Fig. 5 for the two test methods. As expected the number of SEU/h increases with the reactor power. Also the SEU/h in the configuration memory, detected by the SEM controller, is higher than the SEU/h in the BRAMs, detected by the BRAM/ECC sensor. The explanation is the fact that the configuration memory is larger than the BRAM [11]. Moreover the two irradiation tests methodologies had comparable results.

Another important result is the number of unrecoverable errors due to SEU. Fig. 6 shows the errors not repaired by the SEM controller. The BRAM SEU not repaired errors are not shown in Fig. 6 since the sensor implementation cannot distinguish them from the repaired ones (to be implemented on future designs).
Comparing Fig. 5 with Fig. 6 can be seen that the SEM controller not repaired errors are much less than the repaired ones. Nevertheless unrecoverable errors can occur and can lead to FPGA Single Event Functional Interrupts (SEFI), which needs a risk evaluation if used for control purposes in the ITER tokamak.

![Fig. 5. Irradiation tests results of the SEM controller and BRAM SEU sensor for the two test methodologies.](image)

![Fig. 6. SEM controller unrecoverable errors occurred during the irradiation tests.](image)

The ITER data acquisition logic of the FPGA during around 64 hours of tests failed to work with the data acquisition software 13 times. The data acquisition software did not check for errors, this number means only how many times the FPGA stopped to send data to the host that was running the software.

IV. CONCLUSIONS

The performed irradiation tests had neutron fluxes with three orders of magnitude above the ones expected at the ITER port cell cubicles. Yet, the SEM controller was able to repair the majority of the detected SEU errors in the configuration memory. The problematic unrecoverable errors have been relatively few and for the expected neutron flux of ITER this kind of errors will be probably a rare event. Furthermore the configuration memory normally is only partially used and a bit-flip due to a SEU not necessarily means a functional failure. The Virtex-6 FPGA Device Vulnerability Factor (DVF) worst case is 10%, meaning that only 1 in 10 upsets can cause a soft functional error [13].

However unrecoverable errors can occur and preventive mitigation solutions such as firmware redundancy need to be addressed for critical applications.

The BRAM SEU sensors have done only the error detection and respective correction in the memory. This sensor implementation was not able to count the unrecoverable BRAM SEU errors due to architecture limitations (can be improved on future versions). Nevertheless extrapolating from the SEM controller test results is expected that the number of unrecoverable errors in the BRAM memories will be also low, and for the neutron flux of ITER port cell cubicles also a rare event.

Other important consideration is the ITER control cycle versus repair time of SEUs. The control cycle period of tokamak ITER will be as a worst case 1 ms [14] and the time needed to detect/repair an error in one frame of the configuration memory using the SEM controller is around 15 ms, meaning that sixteen control cycles could be not reliable in each repair. In the case of BRAM memory the detect/repair cycle is only 2 μs and probably one control cycle is not reliable when a repair is performed.

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REFERENCES