

Technical Report

# **Analysis of the Effect of Comparator Offset on the ENOB of Charge-Sharing SAR ADCs**

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# Analysis of the Effect of Comparator Offset on the ENOB of Charge-Sharing SAR ADCs

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## Abstract

The charge-sharing (CS) switching scheme appeared recently as an alternative to the charge-redistribution (CR) ADC for moderate-resolution low-power applications. One advantage of the CS is that it requires less demanding reference and input buffers. On the other hand, the CS ADC is very sensitive to the comparator offset, because the latter is translated into non-linearity on the ADC transfer curve. This brief examines the mechanism that causes this non-linearity and proposes a closed-form expression for the maximum effective resolution that a CS ADC may achieve in the presence of comparator offset. Finally, the model is verified with behavioral simulations.

## Index Terms

SAR, ADC, charge-sharing, low-voltage, comparator offset, DNL, INL, ENOB.

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## I. INTRODUCTION

The SAR ADC is very scaling-friendly, since it relies on a highly-digital operation and copes with a rail-to-rail input range without requiring linear amplifiers, which are particularly troublesome to design in modern CMOS processes. While the majority of SAR ADC implementations resort to the charge-redistribution (CR) principle, the SAR ADC based on the charge-sharing (CS) principle appeared recently as an alternative approach [1]. One important distinction between CR and CS SAR architectures is the shape of the current drawn from reference voltage: while the CR SAR interacts with the reference source at each bit decision cycle, the CS SAR draws all the charge required for a conversion from  $V_{\text{ref}}$  in a single cycle and performs the charge processing passively. This characteristic of the CS SAR eases the requirements of the reference generation circuit. Additionally, a SAR ADC that exploits the inherent capacitance of MOS transistors used as capacitors (MOSCAPs) was recently demonstrated [2]. The use of a MOSCAP-based DAC is advantageous because of the higher capacitance density that is provided by these capacitors due to the thin gate dielectric and the automatic availability in digital technologies. On the other hand, the CS ADC is more susceptible to comparator offset, because it causes non-linearity in the ADC transfer curve (in the CR ADC, comparator offset brings only an offset in the transfer curve). This is conventionally overcome through comparator offset voltage compensation [1] or auto-zeroing [3]. While the mechanism that causes this non-linearity is known, no formal analysis or approach to quantify the impact of comparator offset on the effective resolution of CS ADCs is yet reported.

This brief presents an in-depth analysis of the impact of the comparator offset voltage on the linearity of CS SAR ADCs. A closed-form expression for the maximum achievable effective-number-of-bits (ENOB) as function of the comparator offset voltage is proposed, and this model is verified with behavioral simulations. The remaining of this brief is laid out as follows. Section II briefly reviews the CS SAR ADC and derives the models for computation of differential non-linearity (DNL), integral non-linearity (INL) and effective-number-of-bits (ENOB) as function of the comparator offset voltage. Section III compares the model with the results achieved through behavioral simulations. Finally, Section IV presents some design guidelines and concludes this brief.

## II. SUSCEPTIBILITY OF CS-ADCs TO COMPARATOR OFFSET

The conversion procedure of the CS ADC is represented in Fig. 1. A detailed description of the operating principle is out of the scope of this brief, and may be revisited in [1]–[3]. The differential voltage seen by the comparator at the  $i$ -th cycle of the binary search algorithm (where  $i=0$  is the MSB decision) is given by the ratio of the total charge to the total capacitance between nodes P and N. This can be expanded to account for the proportions of the charges and capacitances of the track-and-hold (TH) and DAC, as seen in (1), where  $B$  is the resolution of the ADC,  $V_{\text{in,dif}}$  is the differential input voltage sampled by the TH,  $C_0, C_1, \dots, C_{B-2}$  are the DAC capacitances and  $k_x \in \{0, 1\}$  represent the comparison results, i.e. the digital bits on the ADC output, with  $x \in \{0, 1, \dots, B-1\}$ .

$$V_{\text{PN}} [i] = \frac{\frac{C_{\text{TH}}}{2} V_{\text{in,dif}} - \sum_{j=1}^i (2k_{B-j} - 1) C_{B-j-1} V_{\text{ref}}}{\frac{C_{\text{TH}}}{2} + \sum_{j=1}^i C_{B-j-1}} \quad (1)$$

Because of the summation in the denominator, that indicates that the total capacitance is dynamic, the relationship between charge and voltage is not linear in the CS topology. Ideally, this does not bring any negative impact to the overall ADC linearity, since only the sign of the voltage (positive or negative) is necessary to determine the ADC output binary code. In other words, if the comparator offset voltage is zero, the non-linear relation between charge and voltage in the DAC of the CS ADC does not affect the overall linearity of the converter. However, this particularity is not maintained when the comparator offset voltage is not zero. This may be modeled by inserting a dc voltage source with the magnitude of the input-referred offset  $V_{\text{os}}$  between the DAC and the positive input of the comparator, as shown in Fig. 2. If  $V_{\text{os}}$  is included in the model, the voltage seen by the comparator at any cycle is given by (2).

$$V_{\text{PN}} [i] = \frac{\frac{C_{\text{TH}}}{2} V_{\text{in,dif}} - \sum_{j=1}^i (2k_{B-j} - 1) C_{B-j-1} V_{\text{ref}}}{\frac{C_{\text{TH}}}{2} + \sum_{j=1}^i C_{B-j-1}} - V_{\text{os}} \quad (2)$$

The thresholds of the transitions for different binary codes  $K$ , with  $K = \{k_{B-1} k_{B-2} \dots k_0\}$ , are given in different cycles  $i$ . For example, the mid-scale transition point from 011..1 to 100..0 occurs at the first cycle  $i = 0$ , while the transitions from 0011..1 to 0100..0 and from 1011..1 to 1100..0 happen when  $i = 1$ . Therefore, the cycle  $i$  for which  $V_{\text{PN}} = 0$  for a given code  $K$ , is a

function of  $K$ , or  $i(K)$ . In fact, the value of  $i(K)$  is easily found with the help of (3), where  $l$  is the index of  $k_l$ , and  $k_l$  is the least significant “1” in  $K$ .

$$i(K) = B - 1 - l \quad (3)$$

Differently from what happens with the DAC voltage, the offset voltage is not weighted by the DAC capacitances, causing the non-linear behavior of the ADC. Equaling  $V_{PN}[i]$  to zero and rearranging (2), leads to (4), that denotes the differential input voltage required on the ADC input in order to make a transition to the code  $K$  on the transfer curve. Also, we identify the factor of  $V_{ref}$  as  $\gamma[K]$  and the factor of  $V_{os}$  as  $\eta[K]$ .

$$V_{in,dif}[K] = \underbrace{\frac{\sum_{j=1}^{i(K)} (2k_{B-j} - 1) C_{B-j-1}}{\frac{C_{TH}}{2}}}_{\gamma[K]} V_{ref} + \underbrace{\frac{\frac{C_{TH}}{2} + \sum_{j=1}^{i(K)} C_{B-j-1}}{\frac{C_{TH}}{2}}}_{\eta[K]} V_{os} \quad (4)$$

Thus,  $\gamma[K]$  and  $\eta[K]$  are written as (5) and (6), respectively.

$$\gamma[K] = \frac{2}{C_{TH}} \sum_{j=1}^{i(K)} (2k_{B-j} - 1) C_{B-j-1} \quad (5)$$

$$\eta[K] = 1 + \frac{2}{C_{TH}} \sum_{j=1}^{i(K)} C_{B-j-1} \quad (6)$$

The expression reveals that  $\gamma[k] \cdot V_{ref}$  describes the ideal behavior of a differential ADC and  $\eta[k] \cdot V_{os}$  describes the effect of the comparator offset on the transition point. Also,  $\eta[K]$  is dictated solely by  $i$ , and therefore it is determined by  $B - 1$  unique distinct values, that are arranged in a binary carry sequence [4]. Therefore, in a 3-bit exemple,

$$\eta = \left\{ \eta[1] \ \eta[2] \ \eta[3] \ \eta[4] \ \eta[5] \ \eta[6] \ \eta[7] \right\} \quad (7)$$

can be rewritten as

$$\eta = \left\{ \eta_2 \ \eta_1 \ \eta_2 \ \eta_0 \ \eta_2 \ \eta_1 \ \eta_2 \right\}, \quad (8)$$

where  $\eta_i$  is the value of  $\eta$  for a transition that is determined in the  $i$ -th cycle. It should be noted that (8) is equivalent to (7). Moreover, because of the binary-weighted nature of the DAC capacitance,  $\eta_i$  can be expressed as in (9).

$$\eta_i = 1 + \frac{2^B C_0}{C_{TH}} (1 - 2^{-i}) \quad (9)$$

### A. Differential non-linearity

The differential non-linearity (DNL)  $\delta$  for a given code  $K$  in an ADC with differential input is defined as (10).

$$\delta[K] = \frac{V_{\text{in,dif}}[K+1] - V_{\text{in,dif}}[K]}{V_{\text{LSB}}} - 1 \quad (10)$$

Since  $\gamma[K] \cdot V_{\text{ref}}$  describe the behavior of an ideal ADC, the DNL is only function of  $\eta[K]$  and  $V_{\text{os}}$ , and is reduced to (11).

$$\delta[K] = \frac{\eta[K+1] - \eta[K]}{V_{\text{LSB}}} V_{\text{os}} \quad (11)$$

The largest DNL happens on the MSB transition, since  $\eta_0$  is the minimum and  $\eta_{B-1}$  is the maximum in  $\eta$ . Therefore, the worst DNL is given by (12).

$$|\delta_{\text{max}}| = \frac{2^B C_0}{C_{\text{TH}}} (1 - 2^{-B+1}) \frac{|V_{\text{os}}|}{V_{\text{LSB}}} \quad (12)$$

The DNL is inversely proportional to the ratio between the TH capacitance and the DAC capacitance. Therefore, since the total DAC capacitance  $C_{\text{DAC}}$  is given by (14),

$$C_{\text{DAC}} = (2^{B-1} - 1)C_0 \quad (13)$$

$$= 2^{B-1}C_0 (1 - 2^{-B+1}) \quad (14)$$

we introduce the capacitance ratio  $\alpha$ , defined as (15).

$$\alpha = \frac{C_{\text{TH}}}{2C_{\text{DAC}}} \quad (15)$$

Finally, the DNL expression is simplified to (16).

$$|\delta_{\text{max}}| = \frac{|V_{\text{os}}|}{\alpha V_{\text{LSB}}} \quad (16)$$

It is verified that (11) presents odd-symmetry. Therefore, if (16) returns a value greater than 1 for a given code  $K$ , (9) and (11) would result in  $\delta[K+1]$  or  $\delta[K-1]$  to be lower than -1. By definition, a DNL lower than -1 in the transfer curve of an ADC represents a non-monotonic behavior, while a DNL equal to -1 represents a missing code. In a SAR ADC, the monotonicity is guaranteed by the architecture, preventing the DNL to present values lower than -1. Missing codes, however, are still possible. Therefore, the outcome of a code  $K$  with  $\delta[K]$  larger than 1 is a range of missing codes on the surroundings of  $K$ . This is depicted on the simulated DNL/INL curves in Fig. 3. The range of codes with DNL equaling -1 neighboring a code  $K$  with  $\delta[K] > 1$

is given by  $\lfloor \delta[K] \rfloor$ , where  $\lfloor \cdot \rfloor$  represents the floor function. The absence of missing codes is guaranteed if (17) is verified.

$$|V_{os}| < \alpha V_{LSB} \quad (17)$$

### B. Integral non-linearity

The integral non-linearity (INL) of a code  $K$ , given by  $\phi[K]$ , is proportional to the difference of the actual transition to the transition of a linear best-fit transfer curve, as given in (18).

$$\phi [K] = \frac{V_{in,dif} [K] - V_{in,dif}^{best-fit} [K]}{V_{LSB}} \quad (18)$$

The best-fit transfer curve is found by connecting the endpoints of the actual transfer curve. Thus, solving (4) for the endpoints shows that the transition points of a best-fit transfer curve are given by (19).

$$V_{in,dif}^{best-fit} [K] = \frac{\sum_{j=1}^{i(K)} (2k_{B-j} - 1) C_{B-j-1}}{\frac{C_{TH}}{2}} V_{ref} + \left(1 + \frac{1}{\alpha}\right) V_{os} \quad (19)$$

The second term of (19) represents the offset on the actual ADC transfer curve, caused by the comparator offset, which is given by (20).

$$ADC_{offset} = \left(1 + \frac{1}{\alpha}\right) V_{os} \quad (20)$$

Substituting (4) and (19) into (18) and solving for different values of  $K$  reveals that the  $\phi$  also presents a binary carry sequence pattern. Thus, for a 3-bit example,  $\phi$  is distributed according to (21).

$$\phi = \left\{ \phi_2 \quad \phi_1 \quad \phi_2 \quad \phi_0 \quad \phi_2 \quad \phi_1 \quad \phi_2 \right\} \quad (21)$$

The value of  $\phi_i$ , for any resolution, is given by (22).

$$\phi_i = \left(2^{-B+1} - 2^{-i}\right) \frac{V_{os}}{V_{LSB}} \cdot \frac{2^B C_0}{C_{TH}} \quad (22)$$

The worst-case INL happens for the MSB transition, or  $\phi_0$ , as given in (23).

$$\phi_0 = \left(2^{-B+1} - 1\right) \frac{V_{os}}{V_{LSB}} \cdot \frac{2^B C_0}{C_{TH}} \quad (23)$$

Finally, (23) can be rewritten to include  $\alpha$ , leading to (24).

$$\phi_0 = -\frac{V_{os}}{\alpha V_{LSB}} \quad (24)$$

It is to be noted that (22) and (21) only hold if there are no missing codes in the transfer curve. In order to deal with the enforced monotonicity of the CS ADC, a different method to calculate  $\phi$  in the presence of missing codes must be developed. In this work, this is approached through an alternative definition of  $\phi[K]$ , which is given in (25).

$$\phi[K] = \sum_{j=1}^{K-1} \delta[j] \quad (25)$$

Because of the missing codes surrounding a code with  $\delta[K] > 1$ , a range of values of INL around a missing code  $K$  follows a sequence where the terms are spaced by  $-1$  (e.g.  $\{\dots \phi[K] \phi[K] - 1 \phi[K] - 2 \dots$  and can be approximated by a triangle shape with legs equal to  $|\phi[K]|$ , as seen in Fig. 3. This characteristic is particularly useful on the derivation of the effective resolution in the presence of comparator offset, that follows.

### C. Effective resolution

The quantization noise of an ADC that presents a non-linear transfer curve can be defined by (26) [5], where  $\overline{\phi^2}$  is the mean of the squares of all values in  $\phi$ .

$$V_{\text{noise}}^2 = V_{\text{LSB}}^2 \left( \frac{1}{12} + \overline{\phi^2} \right) \quad (26)$$

The next step assumes that there are missing codes on the transfer curve and that the INL of the code  $K$ ,  $\phi[K]$ , is a positive integer. Exploiting the enforced monotonicity and the shape of  $\phi$ , as already anticipated in the previous subsection, the sum of the values of  $\phi^2$  caused by the non-linearity on the transition to the code  $K$  are given by (27), which represents the sum of the squares of the first  $\phi[K]$  natural numbers.

$$\sum_{j=0}^{\phi[K]} \phi[K + j]^2 = \sum_{i=0}^{\phi[K]} i^2 \quad (27)$$

The expression is further simplified using series identities.

$$\sum_{i=0}^{\phi[K]} i^2 = \frac{\phi[K]^3}{3} + \frac{\phi[K]^2}{2} + \frac{\phi[K]}{6} \quad (28)$$

So far, it is assumed that  $\phi[x]$  is an integer, which is rarely the case. However, it can be shown that (28) provides a very good approximation even when  $\phi[K]$  is not integer. The absolute approximation error  $\epsilon_\phi$  may be computed using (29), where  $\lceil \cdot \rceil$  represents the ceiling function.

$$\epsilon_\phi = \sum_{j=0}^{\lceil \phi[K] \rceil} \phi[K - j]^2 - \left( \frac{\phi[K]^3}{3} + \frac{\phi[K]^2}{2} + \frac{\phi[K]}{6} \right) \quad (29)$$



Fig. 4 shows the resulting value of the sum, together with the error (absolute and relative) caused by the approximation, for  $\phi[x]$  ranging from 0 to  $10V_{LSB}$ . The relative error converges to zero as the value of  $\phi[K]$  grows. While this simplification greatly eases the computations, it is verified that it does not affect significantly the accuracy of the model of ENOB in the presence of comparator offset.

Now, (28) may be used to find the noise contribution of the INL at every transition on the transfer curve. Again, exploiting the symmetry of  $\phi$  (e.g. the  $\phi_1$  code transition pattern happens twice with approximately half the magnitude of  $\phi_0$ ,  $\phi_2$  code transition pattern happens four times with approximately one fourth of the magnitude of  $\phi_0$ , etc, as given by (21) and (22)), the following developments are possible:

$$\overline{\phi^2} = \frac{1}{2^B - 1} \sum_{j=1}^{2^B-1} \phi[j]^2 \quad (30)$$

$$\approx \frac{1}{2^B - 1} \sum_{j=0}^{B-1} \left( 2^j \sum_{m=0}^{\lceil \phi[2^{B-1-j}] \rceil} \phi[2^{B-1-j} + m]^2 \right) \quad (31)$$

$$\approx \frac{1}{2^B - 1} \sum_{j=0}^{B-1} \left( 2^j \left[ \frac{1}{3} \left( \frac{\phi_0}{2^j} \right)^3 + \frac{1}{2} \left( \frac{\phi_0}{2^j} \right)^2 + \frac{1}{6} \left( \frac{\phi_0}{2^j} \right) \right] \right) \quad (32)$$

Expression (32) is further simplified by using geometric series identities, yielding (33).

$$\overline{\phi^2} \approx \frac{1}{2^B - 1} \left[ \frac{4}{9} \phi_0^3 (1 - 2^{-2B}) + \phi_0^2 (1 - 2^{-B}) + \frac{B}{6} \phi_0 \right] \quad (33)$$

For reasonable values of  $B$ ,  $\overline{\phi^2}$  can be approximated by (34).

$$\overline{\phi^2} \approx \frac{1}{2^B} \left( \frac{4}{9} \phi_0^3 + \phi_0^2 + \frac{B}{6} \phi_0 \right) \quad (34)$$

The ENOB is found substituting (34) into (35), which is derived from (26), resulting in (36).

$$\text{ENOB} = B - \log_4 (1 + 12\overline{\phi^2}) \quad (35)$$

$$\text{ENOB} \approx B - \log_4 \left( 1 + 2^{2-B} \left( \frac{4}{9} \phi_0^3 + 3\phi_0^2 + \frac{B}{2} \phi_0 \right) \right) \quad (36)$$

The expression in (36) assumes that the input signal follows a uniform probability distribution. On the other hand, the most common approach to characterize the effective resolution of ADCs uses a sinusoidal test signal. Therefore, following the approach proposed in [5], the scalar correction factor  $\psi$  is used to reconcile the expression with the preferred sinusoidal testing

method. Here,  $\psi$  is the ratio between the INL noise contribution from a sinusoidal distribution and a uniform distribution. In order to estimate the value of  $\psi$ , the INL of a CS ADC with comparator offset is simulated. Then, the average noise power contributed by the INL with a uniformly distributed input is calculated by numerically integrating the curve and normalizing to the code range, finally obtaining  $(\overline{\phi^2})_{\text{uniform}}$ . In order to obtain  $(\overline{\phi^2})_{\text{sinusoid}}$ , the squared INL error is weighted to the probability density function (PDF) of a sinusoid, that is given by (37), where  $K$  represents the output code, and  $K_{\min}$  and  $K_{\max}$  represent the minimum and maximum output codes that are driven by the input signal.

$$\text{PDF}_{\text{sine}}[K] = \frac{1}{\pi \sqrt{(K - K_{\min})(K_{\max} - K)}} \quad (37)$$

The squared INL weighted by the uniform and sinusoidal distributions are shown in Fig. 5, together with the corresponding PDFs. The procedure is mathematically described in (38).

$$\psi = \frac{(\overline{\phi^2})_{\text{sinusoid}}}{(\overline{\phi^2})_{\text{uniform}}} = \frac{\sum_{j=1}^{2^B-1} (\phi[j]^2 \cdot \text{PDF}_{\text{sine}}[j])}{\sum_{j=1}^{2^B-1} (\phi[j]^2 \cdot \frac{1}{2^B-1})} \quad (38)$$

Then, the ENOB expression is rewritten as (39).

$$\text{ENOB} = B - \log_4(1 + 12\psi \overline{\phi^2}) \quad (39)$$

Using  $V_{\text{os}} = 10V_{\text{LSB}}$  and a resolution of 10 bits for the ADC, which are values laid inside a range of practical values, the value of  $\psi \approx 0.67$  is obtained. Finally, the ENOB expression for a CS ADC with comparator offset driven by a sinusoidal input is given by (40), where  $\phi_0$  is given by (24).

$$\text{ENOB} \approx B - \log_4\left(1 + 2^{3-B} \left(\frac{4}{9}\phi_0^3 + \phi_0^2 + \frac{B}{6}\phi_0\right)\right) \quad (40)$$

### III. MODEL VERIFICATION

The model of ENOB versus comparator offset is validated against behavioral simulations. This is done for different combinations of resolution (8, 10 and 12 bits) and  $\alpha$  (0.5, 1, 2, 3, 5). For each combination, the comparator offset voltage is swept from 0 to 10 times the  $V_{\text{LSB}}$  of the 8-bit ADC ( $10 \cdot V_{\text{LSB},8\text{b}}$ ), in a total of 500 linearly spaced steps. For the same input range,  $10 \cdot V_{\text{LSB},8\text{b}}$  is the same as  $40 \cdot V_{\text{LSB},10\text{b}}$  and  $160 \cdot V_{\text{LSB},12\text{b}}$ , and the x-axis of the three plots span the same absolute voltage range, which is approximately 80 mV for a differential input range of 2 V. The simulated ADCs are driven by a sinusoid with peak-to-peak amplitude equal to 95%

of the input range and a dc-offset given by (20), to avoid saturation. The ENOB is extracted from a  $2^{17}$ -point FFT. These results are compared with the results achieved with (40) in Fig. 6. The relative error between the analytical ENOB and the simulated ENOB is found with (41).

$$\epsilon_{\text{ENOB}} = \left( \frac{\text{ENOB}_{\text{analytical}}}{\text{ENOB}_{\text{simulated}}} - 1 \right) \cdot 100\% \quad (41)$$

Fig. 7 plots  $\epsilon_{\text{ENOB}}$  for ADCs with resolutions between 6 and 14 bits,  $\alpha$  between 0.5 and 5, 2 V of input range and an exaggerated range of comparator offset voltage of 0 to 100 mV. The plot reveals that the model is less accurate for low values of  $\alpha$  and low resolutions, because of the assumptions made while calculating  $\psi$ . For resolutions above 8-bits with  $\alpha$  larger than 1,  $|\epsilon_{\text{ENOB}}| < 2\%$ . Interestingly, the ENOB achieved with (40) is slightly pessimistic, despite the approximations used during the derivation.

#### IV. DISCUSSION AND CONCLUSION

In this brief, a model for computing the effective resolution of a CS SAR ADC that has comparator offset was presented. Some important design guidelines can be derived from the analysis: the CS ADC presents missing codes if (17) is not satisfied; the worst-DNL happens at the MSB transition, and is given by (16); the worst-INL also happens at the MSB transition, and is given by (24); the ADC transfer curve presents an offset given by (20); the maximum achievable effective resolution in a CS ADC that has comparator offset is approximated by (40); finally, the capacitance ratio  $\alpha$  can be increased to improve the ADC tolerance to comparator offset, as already pointed out in [2].

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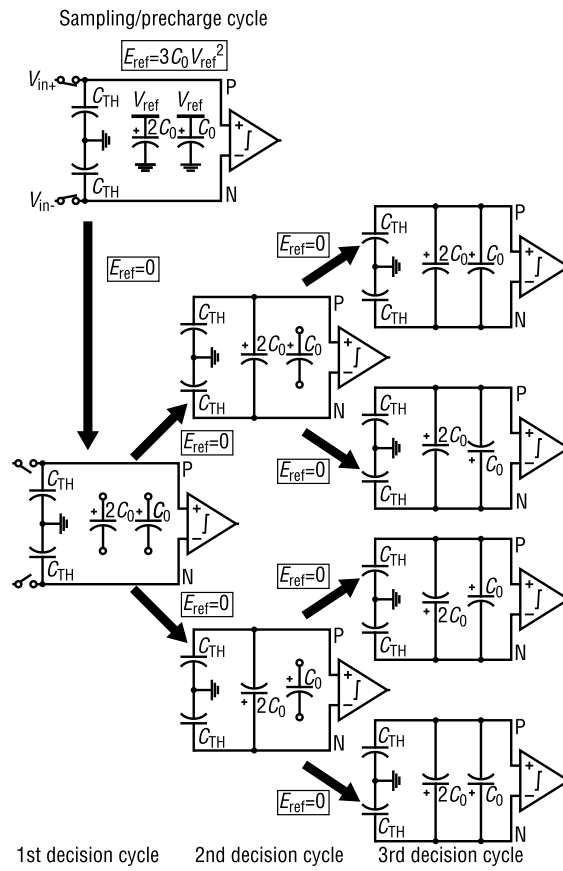


Fig. 1. Schematic and working principle of a 3-bit CS ADC.

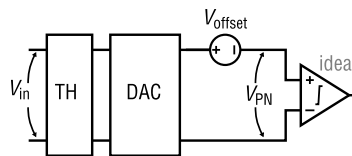


Fig. 2. Circuit for analysis of comparator offset.

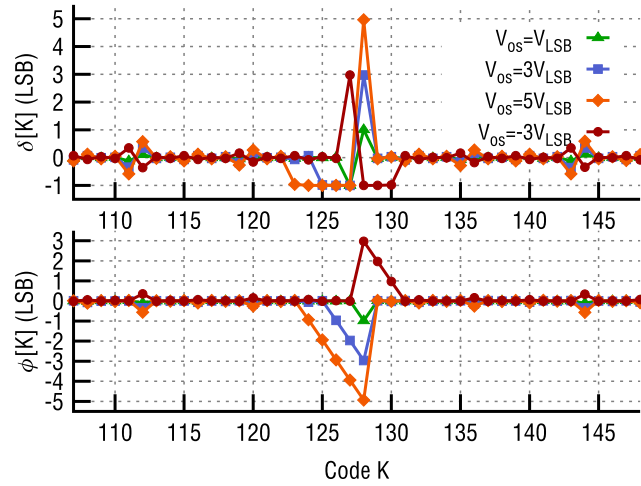


Fig. 3. Simulated DNL and INL curves of an 8-bit CS ADC with different values of comparator offset, zoomed on the MSB transition.

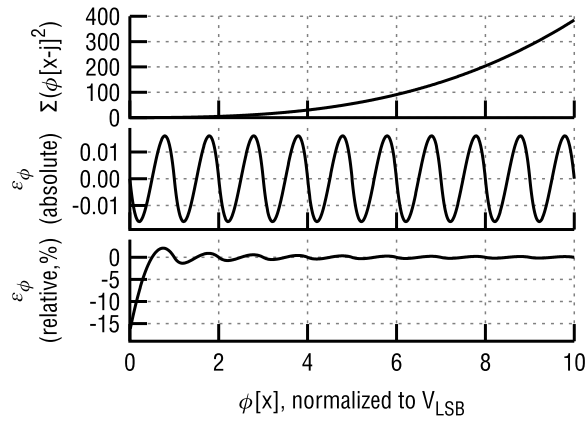


Fig. 4. Absolute and relative error caused by the approximation in (28).

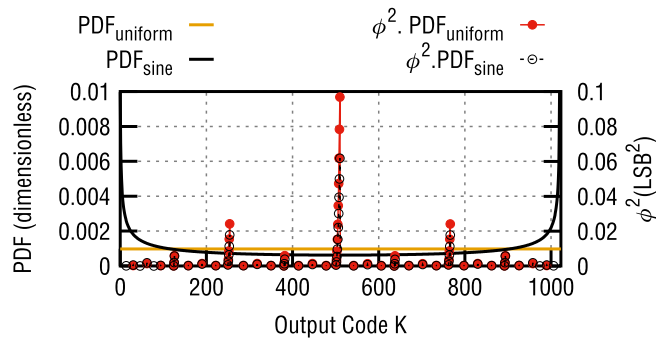


Fig. 5. Left axis: PDFs of uniform and sinusoidal full-range inputs; right axis: squared INL weighted by these PDFs.

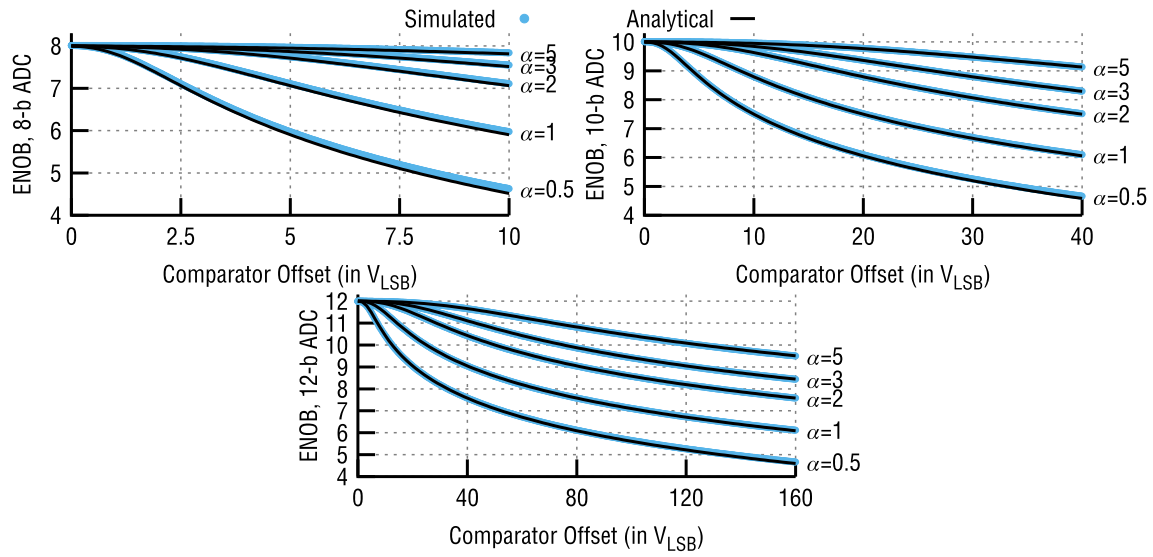


Fig. 6. Comparison between the analytical and simulated ENOB obtained from 500 simulations for each combination of  $B$  and  $\alpha$ , extracted with a  $2^{17}$ -point FFT with a sinusoidal input near Nyquist frequency with 95 % of the full-range.

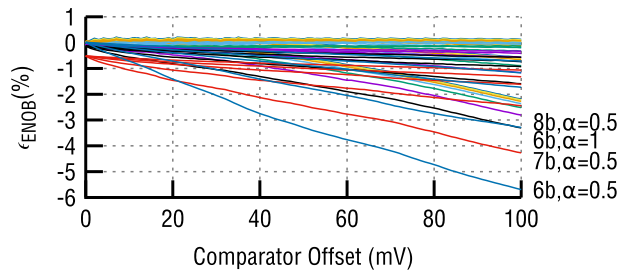


Fig. 7. Plot of  $\epsilon_{ENOB}$  for all resolutions between 6 and 14 bits, with  $\alpha$  ranging from 0.5 to 5, for ADCs with 2 V of input range.