Area-Delay-Power-Aware Adder Placement Method for RNS Reverse Converter Design

Azadeh Alsadat Emrani Zarandi[1], Amir Sabbagh Molahosseini[2], Leonel Sousa[3], Mehdi Hosseinzadeh[1], and Keivan Navi[4]

[1] Department of Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran
E-mail: {a.emrani, hosseinzadeh}@srbiau.ac.ir
[2] Department of Computer Engineering, Kerman Branch, Islamic Azad University, Kerman, Iran
E-mail: sabbagh@iauk.ac.ir
[3] INESC-ID, IST, Universidade de Lisboa, Lisbon, Portugal
E-mail: las@inesc-id.pt
[4] Department of Electrical and Computer Engineering, Shahid Beheshti University, Tehran, Iran
E-mail: navi@sbu.ac.ir

***Abstract*—Residue number systems (RNS) are an attractive alternative to conventional weighted number systems for nowadays applications, due to features such as parallelism and low-power consumption. However, a prerequisite for benefiting from these features is to have a suitable design for *reverse converters*. This paper proposes a practical adder placement method to achieve reverse converters with the desired characteristics based on the target application's requirements and constraints. The presented area-delay-power-aware adder placement method breaks down into four phases. Besides, a linear efficiency function specified for RNS is introduced to choose design with the best trade-off between circuit parameters. The effectiveness of the proposed placement method is experimentally assessed.**

Keywords— Residue number system, reverse converter, adder.

I. INTRODUCTION

Nowadays Very Large Scale Integration (VLSI) designers are mostly focused on reducing power-consumption while improving performance to fulfill portable equipment and wireless world demands. To achieve such ultra-efficient systems, significant arithmetic level improvements should be considered as well as physical level enhancements. Number systems are the pillars for designing arithmetic units. Residue Number Systems (RNS) provide weightless arithmetic with a high-level of parallelism [1].

In the last half century, there have been two major research paths to improve RNS performance: one is focused on the establishment of efficient moduli sets; the other is mainly algorithmic-based, with the aim of achieving simpler formulae, namely by applying modular arithmetic, in order to achieve efficient hardware realizations. Although these two development paths support the progress of RNS and its usage in distinct applications, architecture and hardware-aware methods can make RNS even more powerful with the current moduli sets and the available algorithms. One of these methods was recently introduced in [2] to improve the efficiency of reverse converters. The main idea is to use hardware components with distinct characteristics in specific parts of the system in order to achieve efficiency according to the specifications. However, placing distinct components results in a high variety of structures with distinct characteristics according to circuit parameters and figures of merit such as area, delay and power-consumption. Therefore, the main issue in this approach is to select the design with the optimal trade-off, since there is a large circuit design space.

The aim of this paper is to present an adder placement method that eases the reverse converter design based on the established requirements and constraints. This method includes a step-by-step procedure combining both model-based and implementation aspects to achieve the best area-delay-power-aware design. The implementation results show the capability of this procedure to achieve the best RNS reverse converter design in a large design space, according to the importance and priority of different circuit parameters adjusted by the designer.

II. PLACEMENT PROCEDURE

The placement procedure is presented in Fig. 1, and details about this procedure are provided in the next sub-sections.

A. Moduli Set Considerations

The dynamic range of the RNS can be covered by a larger number of smaller moduli or a lower number of wider moduli. Increasing the number of moduli hampers the reverse converter structure but enhances arithmetic parallelism. The aim of introducing the moduli set evaluation as the first step of this procedure is also to cope with the impact on the reverse converter performance. If the moduli set is not carefully selected, it might not be possible to achieve a reverse converter with the desired characteristics and respecting the required constraints. There will certainly be cases where the selected moduli set results in complex reverse converters, requiring a large number of arithmetic units, namely adders. In those cases, this adder placement procedure can help the designer to achieve

ISBN 978-1-4673-7835-2/16/$31.00©2016 IEEE

IEEE Catalog Number CFP16LAS-ART

structures with the desired circuit characteristics. If the designer wants to operate on a predefined moduli set, he can skip this step of the procedure.

B. Reverse Converter Selection

For the selected moduli set, distinct reverse converter structures can be adopted, and even new structures can be designed.

C. Adder Placement based on Modelling

In this stage, characteristics of components of the selected converter should be analyzed in order to decide which ones are the best candidates for the converter design. First, adder components that fit in the reverse converter architecture should be selected. The result of this step is a configuration table with the different combinations of selected components. It is possible to finish placement at this stage based on a model-based analysis that provides the complexity of the converter, on the target application and on the design goals. However, in more complex situations, it may be desired to restrict even more the possible configurations and therefore facilitate the implementation step. In such cases, further detailed modeling, for example based on the unit-gate model [3], should be pursued. The aim of this step is to estimate the performance of converters with distinct configurations, and to prune the design space by removing configurations with unsuitable estimates.

RNS experts usually place the same type of adder used everywhere in all instances of the same class of circuit to realize all required two-operand additions but the combination of different adder structures on different locations results in better tradeoffs. As it is well known, prefix structures allow obtaining high speed adders at the cost of larger circuit area and power-consumption. The usage of these structures ensemble with others for addition results in a better tradeoff between cost, power and delay. Two main issues should be considered herein: adder components should be selected based on the architecture, and it should be decided where these components are placed. One way of solving these problems is to investigate all possible combinations of different adder placements, and then use them in the next step, or to compare all the estimated values and immediately select the best design. It will certainly be a difficult and time-consuming task, due to the necessity of obtaining and comparing a large set of results.

D. Implementations

The Implementation step covers the specification in hardware description language (HDL) of the various configurations of the reverse converters, preferably by taking advantage of the already available libraries of components, and to verify converters functionality. After synthesis, placing and routing, experimental results in terms of area, delay and power-consumption are gathered for the target technology and can be stored in a database for further use.

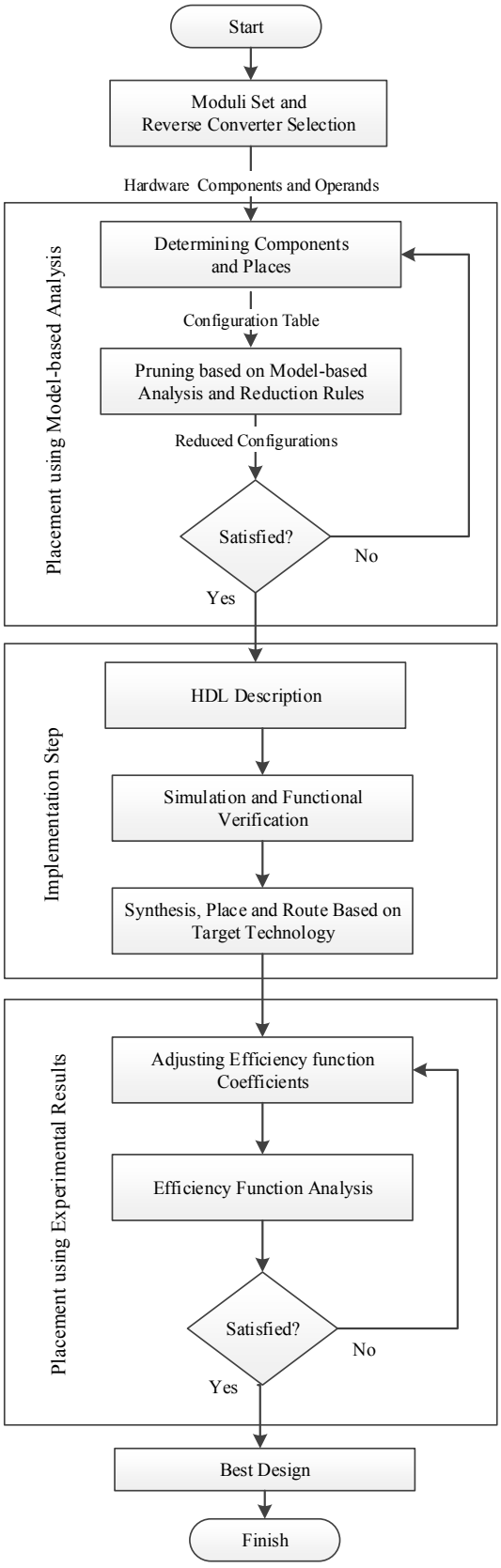

Fig. 1. Block diagram representation of the placement procedure

E. Adder Placement Based on Efficiency Function

As referred, characteristics of components, their placement, and the technology are all parameters with significant impact on the performance and efficiency of RNS reverse converters. Therefore, after the implementation there are converters with a large number of different circuit parameters. The implementation here is done with the purpose of selecting the structure to be used in a real application, to choose the best design based on conditions and requirements. To select the best trade-off it is not an easy task, since there is a large set of parameters and measures involved. Furthermore, depending on the target application the importance of the parameters change. For example, some designs achieve fast converters but at what cost? Is low-speed conversion tolerable for reducing power consumption in a particular cryptographic system? Thus an efficiency function is required to support designers to select the best structure in simple way. Although there are studies about the relationship between different characteristic parameters of integrated circuits, such as the number of external signal connections to a logic block with the number of logic gates in the logic block [4], none of them was able to model the relationship between the delay, the area and the power consumption of a circuit. Herein we propose a simple linear efficiency function (1), which can be used in distinct situations and for different technologies. It should be highlighted that the method proposed in this paper accommodates different efficiency functions, which may accurately model the relation between the distinct variables or address a specific technology.

The linear efficiency function presented in (1) integrates the designer goals, by allowing to assign different relative importance to the various circuits parameters. For example, when power is more important, the designer can give a higher weight to the power consumption. The efficiency function (E) is the inverse of the cost function (E=1/Cost), and is described by the following equation, where C_P, C_D and C_A are coefficients which can take the same value when the importance of all these parameters is the same.

$$E = C_P \frac{Power_{min}}{Power} + C_D \frac{Delay_{min}}{Delay} + C_A \frac{Area_{min}}{Area} \quad (1)$$

However, if the importance of one circuit parameter is greater than the others, it is possible to increase the relative value of the corresponding coefficient. By a matter of normalization, it is suggested to maintain the sum of the coefficients constant: $C_P+C_D+C_A=1$. $Power_{min}$, $Delay_{min}$ and $Area_{min}$ are the lowest power-consumption, delay and area which are achieved among the selected implemented configurations, respectively. E is computed for each implemented configuration by normalizing the values achieved for each parameter by the minimum value, and weighting these values. These quotients influence E in such a way that the higher the value of E, the better the structure (the maximum value for E is one).

The final step of this procedure calculates E considering the defined values for the weights, for all chosen configurations based on the imposed constraints. It should be mentioned that adjusting constraints may need am complete cycle of the design method. In other words, the designer may change them if the required characteristics are not achieved.

III. Case Study: Designing Low-Power Converter

The aim of this section is to design a reverse converter with power-consumption as the main constraint. The moduli set $\{2^n-1, 2^n, 2^n+1, 2^{2n+1}-1\}$ is selected because it is an arithmetic-friendly moduli set with complex reverse conversion. The complex reverse converter helps to illustrate better the proposed placement procedure. After the moduli set selection, the reverse converter is selected and configured. There are different reverse converter structures [5] and [6] suggested for this moduli set and, as it was mentioned before, the target application should also be considered for the selection of the converter structure. Therefore, the first suggested structure [5] is selected due to its lower power-consumption. This structure contains three modulo adders, namely: three CPAs with end-around carry (EAC), one binary CPA, and two CSAs with EACs, as shown in (Fig. 1 of [5]). If we consider all possible components for these four CPAs, the number of different implementations will be high. Therefore, a first pruning based on model-based analysis should be applied to restrict the number of combinations considered.

To investigate the effect of the adder characteristics on the reverse converter performance, adders with different features are selected; some of them are fast, while others require a low-area and less power consumption. It should be noticed that there is a large number of adder structures, and also several combinations are possible. It is not practical to implement all of them. RCAs have the lowest area while it is expected that it consumes the minimum power, but with the lowest speed. We want to achieve a converter with higher speed and almost the same power-consumption, by applying a combination of adders in the reverse conversion structure. We have decided to select three adder components for the CPA-EAC (RCA-EAC, Modulo Prefix [7], HMPE [2]) and also three other for CPA (RCA, Regular Prefix, HRPX [2]). It results in a configuration table with 81 entries, with one different combination of adders per entry. It is not reasonable to implement all these configurations to find out which is the best one. Therefore, it is time to use theoretical analysis to remove unsuitable configurations.

The first pruning stage can be performed by categorizing the required adder components into two groups: those which are on the critical path, and those which are not. Applying a fast adder that has high power-consumption on an uncritical path is not beneficial. The CPA2-EAC of the selected converter is not on the critical path. Therefore, with the aim of achieving a low-power consumption converter, the mentioned adder could be fixed as an RCA-EAC. Just by applying this single step, the number of configurations is reduced from 81 to 27.

The second pruning stage considers the Kogge-Stone method for all the prefix-based component adders to improve

the speed of the fast but even so low-power target converter. It can be seen that the HMPE-Kogge Stone and the Modulo Prefix adders have almost the same area, while the Modulo Prefix is faster. Therefore, from now on, based on the unit-gate model, combinations with HMPE are removed from the configuration options. Even with this pruning there still remain 13 combinations. Since the power-consumption is the major concern in this case study, the third pruning stage consists in withdrawing configurations with two or three prefix-based adders. These designs can be good choices to achieve ultra-high-speed converters, but not for low power. Therefore structures with only one prefix-based adder are kept. This step eliminates 8 further cases. Finally, after considering the above pruning rules and model-based analysis, the five configurations in Table I are reached. In the next step of the application of the proposed method, these cases will be implemented to derive the best design, by evaluating the experimental results and applying the efficiency function proposed. With the purpose of facilitating reading and simplifying the organization of the paper, experimental results for different values of n are presented in [8].

TABLE I
CONFIGURATION TABLE FOR $\{2^n\text{-}1, 2^n, 2^n\text{+}1, 2^{2n+1}\text{-}1\}$ CONVERTER

Cases	CPA1	CPA2	CPA3	CPA4
1	RCA-EAC	RCA-EAC	RCA-EAC	RCA
2	Modulo Prefix	RCA-EAC	RCA-EAC	RCA
3	RCA-EAC	RCA-EAC	Modulo Prefix	RCA
4	RCA-EAC	RCA-EAC	RCA-EAC	Prefix-KS
5	RCA-EAC	RCA-EAC	RCA-EAC	HRPX-KS

Then, placement guided by the efficiency function should be performed in order to determine the best design among the implemented ones, taking into consideration the application constraints. First of all, coefficients of the Efficiency function must be defined. Since our paramount concern in this case study is power-consumption, the largest coefficient is assigned to power (C_P=0.5), the second largest will be delay (C_D=0.3), and finally area (C_A=0.2). Table II presents the obtained values for the efficiency function for two technologies. It is noted that the greater the value of the efficiency function, the better the design is, with the optimal value 1. It can be seen that with the 65nm technology, the design 2 is selected as the best. It does not reach the minimum power-consumption, however it has the best balance between power-consumption and speed. For instance, for n=16, the design 2 achieved 13 and 8 percent delay and area savings, respectively, while only 5 percent of the power is reduced [8]. Therefore, the design 1 [5], with an architecture nowadays prevalent in converter design, is not a good "low-power converter", since to achieve the smallest power-consumption it significantly degrades the other circuit parameters. On the other hand, in 90 nm technology the 5 is the best design, and the efficiency function becomes one for all values considered for n. This shows that an adder component specifically designed for reverse converters, HRPX, can effectively result in better performance. It also stresses the fact that technology is one of the key factors for determining the best design. Hence, our procedure combines both model-based and experimental aspects to achieve the best reverse converter for a given technology. When selected designs satisfy the defined constraints, procedure is finished.

TABLE II
EFFICIENCY FUNCTION VALUES FOR MODULI SET $\{2^n\text{-}1, 2^n, 2^n\text{+}1, 2^{2n+1}\text{-}1\}$ CONVERTERS

Case	TSMC 65nm				UMC 90nm			
	4	8	12	16	4	8	12	16
1-1	0.941	0.891	0.892	0.882	0.782	0.801	0.775	0.814
1-2	0.964	0.892	0.895	0.906	0.767	0.814	0.813	0.741
1-3	0.942	0.775	0.726	0.719	0.653	0.738	0.690	0.713
1-4	0.870	0.792	0.753	0.731	0.675	0.681	0.647	0.633
1-5	0.897	0.828	0.780	0.749	1	1	1	1

IV. CONCLUSIONS

This paper presents an adder placement method that considers both model-based and experimental analysis to achieve the best hardware reverse converter design based on different aspects and requirements. This procedure consists of two major parts: *i*) the first part is independent of the technology, by considering a model-based analysis and suggested rules; *ii*) the second part is takes in consideration the technology and makes use of an Efficiency function to determine the best design using a specific implementation technology. It is shown that this procedure is able to benefit from every adder components, even future ones, and their different combinations to improve the available and future RNS reverse converter designs.

REFERENCES

[1] A. Omondi and B. Premkumar, *Residue Number Systems: Theory and Implementations*, Imperial College Press, London, 2007.

[2] A.A.E. Zarandi, A.S. Molahosseini, M. Hosseinzadeh, S. Sorouri, S. Antao, and L. Sousa, "Reverse Converter Design via Parallel-Prefix Adders: Novel Components, Methodology and Implementations," *IEEE Trans. VLSI Syst.,* vol. 23, no. 2, pp. 374-378, 2015.

[3] R. Zimmermann, "Binary Adder Architectures for Cell-Based VLSI and Their Synthesis," PhD Thesis, ETH Zurich, Switzerland, 1997.

[4] P. Christie, D. Stroobandt, "The Interpretation and Application of Rent's Rule," *IEEE Trans. VLSI Syst.*, vol. 8, no. 6, pp. 639–648, 2000.

[5] A.S. Molahosseini, K. Navi, C. Dadkhah, O. Kavehei, S. Timarchi, "Efficient Reverse Converter Designs for the New 4-Moduli Sets $\{2^n\text{–}1, 2^n, 2^n\text{+}1, 2^{2n+1}\text{-}1\}$ and $\{2^n\text{-}1, 2^n\text{+}1, 2^{2n}, 2^{2n}\text{+}1\}$ Based on New CRTs," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 4, pp.823-835, 2010.

[6] L. Sousa and S. Antão, "MRC-based RNS Reverse Converters for the Four-Moduli Sets $\{2^n\text{+}1, 2^n\text{-}1, 2^n, 2^{2n+1}\text{-}1\}$ and $\{2^n\text{+}1, 2^n\text{-}1, 2^{2n}, 2^{2n+1}\text{-}1\}$," *IEEE Trans. Circuits Syst. II*, vol. 59, no. 4, pp. 244-248, 2012.

[7] R.A. Patel, M. Benaissa and S. Boussakta, "Fast Parallel-Prefix Architectures for Modulo 2^n-1 Addition with a Single Representation of Zero," *IEEE Trans. Comput.*, vol. 56, no. 11, pp. 1484-1492, 2007.

[8] A.A.E. Zarandi, A.S. Molahosseini and L. Sousa, "ASIC and FPGA Implementations of Modern 4-Moduli RNS Reverse Converters Using Distinct Configurations," Instituto de Engenharia de Sistemas e Computadores (INESC-ID) Technical Report 8/2015, Portugal, Mar. 2015 (http://www.inesc-id.pt/ficheiros/publicacoes/11002.pdf).