Solid State Bipolar Marx Modulators: Overvoltage Tolerance Capability

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***Abstract*—Two solid-state bipolar Marx modulators are compared in terms of semiconductors overvoltage tolerance capability in abnormal operating conditions such as switching synchronization failure. Simulation results are presented for 4 stages of two Marx circuits using 500 V per stage with 1 kHz bipolar pulse repetition rate, with 5 µs pulse width and 10 µs relaxation time into resistive load.**

I. INTRODUCTION

Through the years, power semiconductors increased their importance in pulsed power topologies named the Marx generator, conferring flexibility, higher pulse frequency and duty cycle, [1-5]. The increase of interest, for instance, from food and water purification industry applications for compact modulators and for bipolar pulses led to development of solid-state bipolar Marx modulators, [6-10]. However, in one hand topologies with additional switches for fault capability require complex triggering circuit on another hand optimized topologies, with reduced number of switches in each cell, uses some switches for more than one operating mode, contributing to the lack of current modularity of Marx type circuits, [11]. Aggravating this feature, the parallel charging technique increases the current in charging switches that are near the power supply [12]. Thus, when designing a solid-state Marx modulator, power semiconductors selection is also to be considered, not only by current rating but also by overvoltage across the switches in abnormal switching operation among operating modes.

The purpose of this paper is to present an analysis of semiconductors voltages in two solid-state bipolar Marx modulators presented in Fig. 1, under failure condition such as switch synchronism failure and open fault, considering that the semiconductors remain open-circuited when defective.

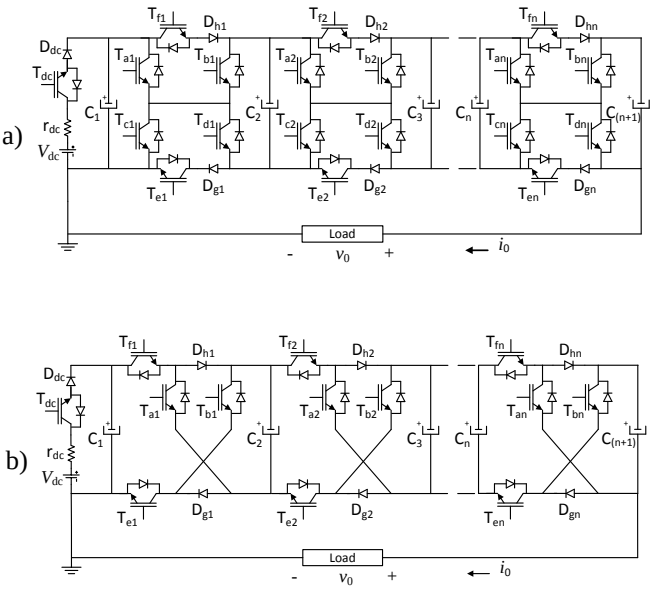


Fig. 1. Bipolar solid-state Marx modulators topologies, a) generalized with 6 on-off semiconductors and b) optimized, with 4 semiconductors on-off, per stage.

II. SEMICONDUCT'S VOLTAGE

Fig. 1 presents two solid-state bipolar Marx modulators, having each with *n* stages, with IGBTs as on-off switches as described in detail elsewhere [8-9]. The main three operating modes of circuits of Fig. 1 are summarized in Table I. For clearness the IGBT anti-parallel diodes are not labelled in the circuits of Fig. 1, being named after the IGBT device number (e.g., D_{a1} corresponds to the anti-parallel diode of IGBT T_{a1}).

TABLE I

SEMICONDUCTORS'TURNED ON OF THE CIRCUITS OF FIG. 1 FOR CHARGING AND PULSE OPERATING MODES

Circuit	Operating mode		
	Charging	Positive Pulse	Negative Pulse
Fig. 1a)	T_{fi} & T_{ei} or T_{ai} & D_{bi} & T_{ei} or T_{fi} & D_{di} & T_{ci}	T_{ai} & T_{di}	T_{bi} & T_{ci}
Fig. 1b)	T_{fi} & T_{ei}	T_{fi} & T_{ai}	T_{bi} & T_{ei}

The solid-state bipolar Marx modulators presented in Fig. 1 and the switch path for charging and pulse operating modes shown in Table I are considered. Also, the collector to emitter switch ON voltage and anode-cathode voltage of ON diodes are considered to be approximately zero. The following sections will present an analysis of the switch voltages in the circuits of Fig. 1 under faulty condition such as switch synchronization failure (leading to brief open faults).

1) Charging the capacitors

Considering the circuit of Fig. 1a) and in case of synchronization failure (delay) of switch T_{fi} or T_{ei} of any independent (i) stage, the hold-off voltage across the delayed switch is the difference between voltages of capacitors C_i and C_{i+1}, $V_{C_i} - V_{C_{i+1}}$. In case of failure of both T_{fi} and T_{ei} switches, these switches share the above voltage difference. In any of these individual or simultaneous switch failures, the set of switches T_{ai} and T_{ci} or switches T_{bi} and T_{di} share the voltage of V_{C_i} or $V_{C_{i+1}}$, respectively, as listed in Table II. Considering now the circuit of Fig. 1b), similar situation happens in case of individual or simultaneous failure of switches T_{fi} and T_{ei}, as shown in Table II.

2) Positive pulse

Considering circuit of Fig. 1a) in positive pulse operating mode, and considering delays in switches T_{ai} or/and T_{di}, these switches hold-off the voltage of V_{dc} in case of individual or simultaneous failure as listed in Table II. However, this is different for circuit of Fig. 1b), because the failure of switch T_{fi} implies that this delayed switch has to sustain a voltage nearly equal two times the power supply voltage, i.e. $2V_{dc}$. Considering yet the circuit of Fig. 1b) and for situations of individual failure of switch T_{ai} or simultaneous failure of switches T_{fi} and T_{ai}, the delayed switch(es) hold-off the V_{dc} voltage, as shown in Table II.

TABLE II

FAULT CLEARANCE PATH AND HOLD-OFF VOLTAGE OF SEMICONDUCTORS FOR CHARGING AND PULSE OPERATING MODES OF THE CIRCUITS OF FIG. 1 AND THE OUTPUT VOLTAGE UNDER FAULT CONDITION

Operat. mode	Circuit	Switch in fault condition	Hold-off voltage of faulty switches	Hold-off voltage of switches in OFF-state driven
Charg.	Fig. 1a)	T_{fi}	$V_{CE_{T_{fi}}} = V_{C_i} - V_{C_{i+1}}$	$V_{CE_{T_{ai}}} + V_{CE_{T_{ci}}} = V_{C_i}$ and $V_{CE_{T_{bi}}} + V_{CE_{T_{di}}} = V_{C_{i+1}}$
		T_{ei}	$V_{CE_{T_{ei}}} = V_{C_i} - V_{C_{i+1}}$	
		T_{fi} & T_{ei}	$V_{CE_{T_{fi}}} + V_{CE_{T_{ei}}} = V_{C_i} - V_{C_{i+1}}$	
	Fig. 1b)	T_{fi}	$V_{CE_{T_{fi}}} = V_{C_i} - V_{C_{i+1}}$	$V_{CE_{T_{ai}}} = V_{C_{i+1}} + V_{AK_{D_{hi}}}$ and $V_{CE_{T_{bi}}} = V_{C_{i+1}} + V_{AK_{D_{gi}}}$
		T_{ei}	$V_{CE_{T_{ei}}} = V_{C_i} - V_{C_{i+1}}$	
		T_{fi} & T_{ei}	$V_{CE_{T_{fi}}} + V_{CE_{T_{ei}}} = V_{C_i} - V_{C_{i+1}}$	
Pos. pulse	Fig. 1a)	T_{ai}	$V_{CE_{T_{ai}}} = V_{dc}$	$V_{CE_{T_{bi}}} \approx V_{dc}$ $V_{CE_{T_{ci}}} = V_{CE_{T_{di}}} = V_{CE_{T_{ei}}} = V_{CE_{T_{fi}}} \approx 0$ $V_{AK_{D_{gi}}} = V_{AK_{D_{hi}}} \approx 0$
		T_{di}	$V_{CE_{T_{di}}} = V_{dc}$	$V_{CE_{T_{ci}}} \approx V_{dc}$ $V_{CE_{T_{ai}}} = V_{CE_{T_{bi}}} = V_{CE_{T_{ei}}} = V_{CE_{T_{fi}}} \approx 0$ $V_{AK_{D_{gi}}} = V_{AK_{D_{hi}}} \approx 0$
		T_{ai} & T_{di}	$V_{CE_{T_{ai}}} = V_{CE_{T_{di}}} = V_{dc}$	$V_{CE_{T_{ei}}} \approx 0$ $V_{CE_{T_{fi}}} \approx V_{dc}$ $V_{AK_{D_{gi}}} \approx -V_{dc}$ $V_{AK_{D_{hi}}} \approx 0$
	Fig. 1b)	T_{fi}	$V_{CE_{T_{fi}}} = 2V_{dc}$	$V_{CE_{T_{ai}}} = V_{CE_{T_{bi}}} = V_{CE_{T_{ei}}} \approx 0$ $V_{AK_{D_{gi}}} \approx -V_{dc}$ $V_{AK_{D_{hi}}} \approx -V_{dc}$
		T_{ai}	$V_{CE_{T_{ai}}} = V_{dc}$	$V_{CE_{T_{bi}}} + V_{CE_{T_{ei}}} \approx V_{dc}$ $V_{CE_{T_{fi}}} \approx 0$ $V_{AK_{D_{gi}}} = V_{CE_{T_{bi}}} - V_{dc}$ $V_{AK_{D_{hi}}} \approx 0$
		T_{fi} & T_{ai}	$V_{CE_{T_{fi}}} + V_{CE_{T_{ai}}} = 2V_{dc}$	$V_{CE_{T_{bi}}} = V_{CE_{T_{ei}}} \approx 0$ $V_{AK_{D_{gi}}} \approx -V_{dc}$ $V_{AK_{D_{hi}}} = V_{CE_{T_{bi}}} - V_{dc}$
Neg. pulse	Fig. 1a)	T_{bi}	$V_{CE_{T_{bi}}} = V_{dc}$	$V_{CE_{T_{ai}}} \approx V_{dc}$ $V_{CE_{T_{ci}}} = V_{CE_{T_{di}}} = V_{CE_{T_{ei}}} = V_{CE_{T_{fi}}} \approx 0$ $V_{AK_{D_{gi}}} = V_{AK_{D_{hi}}} \approx 0$
		T_{ci}	$V_{CE_{T_{ci}}} = V_{dc}$	$V_{CE_{T_{di}}} \approx V_{dc}$ $V_{CE_{T_{ai}}} = V_{CE_{T_{bi}}} = V_{CE_{T_{ei}}} = V_{CE_{T_{fi}}} \approx 0$ $V_{AK_{D_{gi}}} = V_{AK_{D_{hi}}} \approx 0$
		T_{bi} & T_{ci}	$V_{CE_{T_{bi}}} = V_{CE_{T_{ci}}} = V_{dc}$	$V_{CE_{T_{ei}}} \approx V_{dc}$ $V_{CE_{T_{fi}}} \approx 0$ $V_{AK_{D_{gi}}} \approx 0$ $V_{AK_{D_{hi}}} \approx -V_{dc}$
	Fig. 1b)	T_{bi}	$V_{CE_{T_{bi}}} = V_{dc}$	$V_{CE_{T_{ai}}} + V_{CE_{T_{fi}}} \approx V_{dc}$ $V_{CE_{T_{ei}}} \approx 0$ $V_{AK_{D_{gi}}} \approx 0$ $V_{AK_{D_{hi}}} = V_{CE_{T_{ai}}} - V_{dc}$
		T_{ei}	$V_{CE_{T_{ei}}} = 2V_{dc}$	$V_{CE_{T_{ai}}} = V_{CE_{T_{bi}}} = V_{CE_{T_{fi}}} \approx 0$ $V_{AK_{D_{gi}}} \approx -V_{dc}$ $V_{AK_{D_{hi}}} \approx -V_{dc}$
		T_{bi} & T_{ei}	$V_{CE_{T_{bi}}} + V_{CE_{T_{ei}}} = 2V_{dc}$	$V_{CE_{T_{ai}}} = V_{CE_{T_{fi}}} \approx 0$ $V_{AK_{D_{gi}}} = V_{dc} - V_{CE_{T_{bi}}}$ $V_{AK_{D_{hi}}} \approx -V_{dc}$

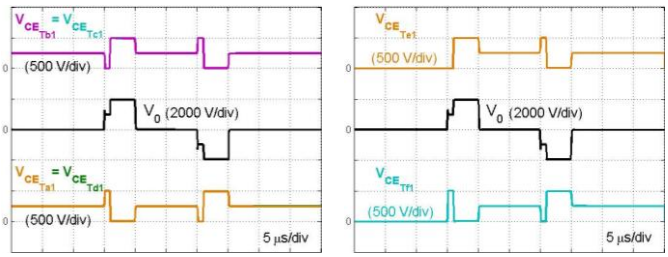
3) Negative pulse

To apply negative pulse in circuit of Fig. 1a), switches T_{bi} and T_{ci} are turned ON. However, if any of these switches in each independent stage individually or simultaneously fails to turn ON the hold-off of voltage of faulty switch or switches is V_{dc}, as shown in Table II. This voltage condition is similar to the circuit of Fig. 1b) in case of failure switch T_{bi} or simultaneous switches T_{bi} and T_{ei}, but it is not verified in case of individual failure of switch T_{ei}, as this switch has to hold-off the V_{dc} voltage, as illustrated in Table II.

III. Simulation Results

The circuit of Fig. 1, with four stages was simulated in SIMULINK, MATLAB software. The simulated circuit was operated with V_{dc} ~500 V, 1 kHz, and 5 µs pulses width. The switch synchronism failure was simulated by delaying 1 µs to turn ON switches, T_a, T_b, T_c, and T_d of the first stage in regard of other stages switches.

In Fig. 6 are shown the simulated results for switches: a) T_{a1}, T_{b1}, T_{c1} and T_{d1}, and b) T_{e1} and T_{f1}, voltages, during normal charging and abnormal pulse (positive and negative) operating modes.



(a) (b)

Fig. 6 – Simulation results for the hold-off voltage of switches of the circuit of Fig. 1a) with lack of synchronism of simultaneous switches T_{a1} and T_{d1} for positive pulse and T_{b1} and T_{c1} for negative pulse: a) switches T_{a1}, T_{b1}, T_{c1} and T_{d1} hold-off voltage and the output voltage; b) switches T_{e1} and T_{f1} hold-off voltage and the output voltage. The scales are 5 µs/div (horizontal) and 500 V/div (vertical).

Considering Fig. 6a) and during charging operating mode, the set of switches T_{a1} and T_{d1} or T_{b1} and T_{c1} shares the voltage of V_{dc}. Considering pulse operating mode, and during the lapse of synchronism of switches T_{a1} and T_{d1} or T_{b1} and T_{c1} for positive and negative pulse, respectively, these switches hold-off the V_{dc} voltage accordingly to section II. Regarding switches T_{e1} and T_{f1} (Fig. 6b)), during negative delayed condition, switch T_{e1} holds-off the V_{dc} voltage, but the voltage across switch T_{f1} is approximately zero, because the anti-parallel diode D_{f1} is forward biased. This is similar for switches T_{a1} and T_{d1} for abnormal positive pulse condition, as these switches hold-off a voltage of V_{dc} and switch T_{f1}, but

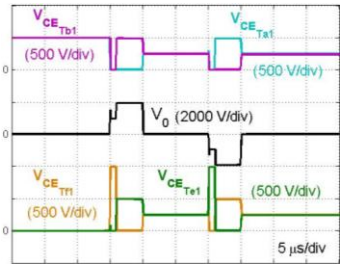


Fig. 7 – Simulation results for the hold-off voltage of switches T_{a1}, T_{b1}, T_{e1} and T_{f1} of the circuit of Fig. 1b) with lack of synchronism of switches T_{f1} and T_{e1} for positive pulse and negative pulse, respectively. The scales are 5 µs/div (horizontal) and 500 V/div (vertical).

switch T_{e1} voltage is zero, due to the anti-parallel diode D_{e1} becomes forward biased.

Fig. 7 shows the simulated waveforms for hold-off voltage of switches T_{a1}, T_{b1}, T_{e1} and T_{f1} during different operating modes and the output voltage of circuit of Fig. 1b). Considering charging period, switches in OFF-state (T_{a1} and T_{b1}) hold-off a voltage of V_{dc}, as described in section II. In negative pulse operating mode and during synchronization failure of switch T_{e1}, this switch has to hold off the double ($2V_{dc}$) of the V_{dc} voltage while the switches T_{a1} and T_{f1} voltage is approximately zero because the anti-parallel diodes D_{a1} and D_{f1} are forward biased. This situation is analogous for switch T_{f1} with respect of lack of synchronism during positive pulse operating mode, where the switch T_{f1} has to hold-off the voltage of $2V_{dc}$ and the voltage across the OFF-state driven switches T_{b1} and T_{e1} is approximately zero, as can be seen in Fig. 7.

IV. Conclusions

A comparative analysis of two solid-state Marx modulators was presented in terms of hold-voltage in abnormal switching operating condition such as switching synchronization failure.

Simulation results shows that in circuit of Fig. 1a) the maximum hold-off voltage of any switch within fault condition is V_{dc} against the hold-voltage of $2V_{dc}$ for faulty switches T_{f1} and T_{e1} of circuit of Fig. 1b) for positive and negative operating mode, respectively, presenting a hold-off voltage asymmetry between semiconductors at the same stage.

V. Acknowledgements

This work was supported by national funds through Fundação para a Ciência e a Tecnologia (FCT) with reference UID/CEC/50021/2013.

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